Insights to the Scaling Impact on Back-Gate Biasing for FD SOI MOSFETs

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Abstract — This work investigates the scaling impact on the feasibility of back-gate biasing for ultra-thin-body and BOX fully depleted SOI MOSFETs (UTBB FD SOI) at 5nm technology node. Though the effectiveness of the threshold voltage ($V_t$) modulation by back bias is limited due to bulk inversion as a result of silicon film scaling, such an issue of reduced $V_t$ window can be relieved by decreasing BOX thickness as the back-gate coupling could be enhanced by thin-BOX-reduced inversion charge centroid in scaled SOI film.

Keywords — FD SOI, ultra-thin body and box (UTBB), back bias.

Device Simulation and Design

Following ITRS rules at 5nm technology node, the FD-SOI is designed by Sentaurus TCAD. Undoped channel and highly doped ground plane are used.

![Fig. 1 Conceptual schematic of FD-SOI (not to scale).](image)

Drain-induced barrier lowering (DIBL) can be controlled with scaled $T_{BOX}$ and highly doped GP by suppressing the penetration of the fringing electric field.

With sufficiently thin $T_{Si}$, the subthreshold swing (SS) increases as $T_{BOX}$ decreases due to smaller contribution of front gate capacitance (1-D effect). On the contrary, the lateral electrical field becomes apparent and can be suppressed with thin $T_{BOX}$ when $T_{Si}$ approaches $L_0$, such that SS starts to decrease with $T_{BOX}$ decreasing (2-D effect).

Back-Gate Bias Technique

The flexibility of the back bias technique is explored herein for UTBB SOI at 5nm technology. When a forward bias is applied to the back gate, the threshold voltage is lowered due to coupling from the back gate.

![Fig. 2 TCAD- and macro model-predicted (a)read voltage transfer characteristics (b)write current for the 6T-SRAM.](image)

![Fig. 4 (a) $V_t$ operation window versus $T_{Si}$ with $T_{BOX} = 10$nm. (b) $V_t$ operation window versus $T_{Si}$ with various $T_{BOX}$.](image)

Since $T_{Si}$ scaling is needed for good control of SCEs, it is necessary for decreasing $T_{BOX}$, which can not only enhance the $V_t$ tuning window but also reverse the dependence on $T_{Si}$ scaling for the thinnest $T_{BOX}$.

The sensitivity of $V_t$ to $V_{GSS}$ can refer to the coupling factor: $r = \frac{3EOT \times x_c}{3T_{BOX} + T_{Si} \times x_c}$

where $x_c$ is the inversion charge centroid position

The $x_c$ position is determined by the front-gate and back-gate, and $x_c$ increases with back bias, resulting in larger coupling effect, especially for thicker $T_{Si}$.

![Fig. 5 (a) Inversion charge centroid position and (b) coupling factor versus $T_{Si}$ with different $T_{BOX}$ ($V_{GSS} = 0$V).](image)

To continue to maintain the $V_t$ flexibility using back bias for 5nm node and beyond, $T_{BOX}$ should also be scaled accordingly.

Conclusion — The device scaling impact on the feasibility of back-gate biasing for FD SOI at 5nm technology node has been investigated. Though the common scaling rule suggests that the $V_t$ flexibility using back bias is limited by bulk inversion, the back bias technique is still found to be viable if the BOX thickness is scaled accordingly. The thin-BOX-reduced inversion charge centroid in scaled SOI film is beneficial to back-gate coupling.