A 60-GHz High-Gain, Low-Power, 3.7-dB Noise-Figure Low-Noise Amplifier in 90-nm CMOS

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**KEYNOTE:**

1. Two-stage cascade structure with a common-source buffer amplifier.
2. Inter-stage noise matching inductor + derivative superposition (DS) method – Good NF & linearity
3. Max. gain: 22 dB @ 57.3 GHz
4. Min. NF: 3.7 dB @ 61 GHz
5. Power consumption: 13.5 mW

**FOM**

\[ FOM = \frac{G_{in}}{1 + \frac{F_{IP1dB}}{F_{IIP3}}} \]

- **NF Improvement**: 4.9 to 3.7 dB @ 60 GHz
- **TFMS spiral inductors** (more layout flexibility)
- **First two stage current density**: 156 \( \mu \)A/\mu m
- **L_m** resonates \( C_{dss} \) & \( C_{gs2} \) (\( L_m=0.17 \) nH, \( Q=16 \))
- **NF improvement**: 4.9 to 3.7 dB @ 60 GHz
- **IP1dB**: -23 dBm & **IIP3**: -12 dBm @ 60 GHz
- **IRL & ORL** are well below -10 dB @ 57 - 64 GHz

**PERFORMANCE COMPARISON**

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (CMOS)</th>
<th>Supply Voltage (V)</th>
<th>Topology</th>
<th>Gain (dB)</th>
<th>IIP3 (dBm)</th>
<th>IP1dB (dBm)</th>
<th>NFmin (dB)</th>
<th>Power (mW)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010 IMS</td>
<td>0.13 ( \mu )m</td>
<td>1.5</td>
<td>Current-reused</td>
<td>13.2 @ 58 GHz</td>
<td>-4.7</td>
<td>-15</td>
<td>4.9</td>
<td>29.1</td>
<td>6.8</td>
</tr>
<tr>
<td>2011 MWCL</td>
<td>0.13 ( \mu )m</td>
<td>1.5</td>
<td>3-stage cascode</td>
<td>21 @ 53 GHz</td>
<td>-16</td>
<td>-25</td>
<td>8.3</td>
<td>15.1</td>
<td>1.9</td>
</tr>
<tr>
<td>2011 RFIC</td>
<td>65 nm</td>
<td>1.2</td>
<td>3-stage cascode (with T-Line)</td>
<td>20.6 @ 60 GHz</td>
<td>N/A</td>
<td>-29</td>
<td>4.9 @ 58 GHz</td>
<td>33.6</td>
<td>–</td>
</tr>
<tr>
<td>2012 RFIC</td>
<td>65 nm</td>
<td>1.25</td>
<td>3 CS TF + CF</td>
<td>23 @ 60 GHz</td>
<td>-16.5</td>
<td>-26.5</td>
<td>4</td>
<td>8</td>
<td>22.2</td>
</tr>
<tr>
<td>This Work</td>
<td>90 nm</td>
<td>1.5</td>
<td>2-stage cascode + 1 CS</td>
<td>22 @ 57.3 GHz</td>
<td>-13</td>
<td>-23</td>
<td>3.7 @ 61 GHz</td>
<td>13.5</td>
<td>25.4</td>
</tr>
</tbody>
</table>

**Chip size**: 0.76x0.78 mm\(^2\)

**CIRCUIT DESIGN**

- **Lm (nH)**
- **SCLLSI**
- **TFMS spiral inductors** (more layout flexibility)
- **Noise considerations**
- **Linearity considerations**