A 60-GHz High-Gain, Low-Power, 3.7-dB Noise-Figure Low-Noise Amplifier in 90-nm CMOS

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Abstract — This paper presents a 60-GHz high-gain, low-power, 3.7-dB noise-figure (NF), CMOS low-noise amplifier (LNA) fabricated with a 90-nm process. The CMOS LNA exhibited a two-stage cascode structure with a common-source buffer amplifier. To achieve a lower NF and to prevent poor linearity, an inter-stage noise matching inductor and a derivative superposition method were applied to the LNA design. A thin-film microstrip (TFMS) line was used for matching networks and all interconnections. The TFMS line consists of a top metal layer (M9) serving as the signal microstrip line and a bottom metal layer (M1) serving as the ground plane. The measurement results showed that the proposed LNA exhibited the best gain performance of 22 dB at 57.3 GHz and a minimum NF of 3.7 dB at 61 GHz. The input third-order intercept point was -13 dBm. Further, the proposed LNA dissipated a total power of 13.5 mW from a 1.5 V power supply.

Index Terms — 60-GHz, derivative superposition, low-noise amplifier (LNA), noise matching, thin-film microstrip (TFMS) line.

I. INTRODUCTION

In recent years, the V-band spectrum for wireless personal network (WPAN) applications has become of special interest owing to its bandwidth of approximately 7 GHz, centered around 60 GHz. A high-quality, millimeter-wave (MMW), low-noise amplifier (LNA) plays an important role in modern wireless communication systems. In order to realize low-cost integration of the baseband and the RF front-end on the same die, a complementary metal-oxide semiconductor (CMOS) technology is one of the most attractive solutions to implement a highly integrated systems-on-chip (SoC) for MMW communication applications.

In the case of the LNA design in MMW receivers, an amplifier with a multistage topology is generally adopted to increase the power gain. However, the DC power consumption of such an amplifier is relatively high [1]. A gate-inductive gain-peaking technique for the LNA design [2] is an effective way to achieve high gain performance with low power. Unfortunately, a high gain amplifier suffers from poor linearity. To improve the linearity properties, [3]-[5] have been studied. However, in these works, high linearity and a low noise figure (NF) could not be achieved simultaneously.

In this paper, we present a 60-GHz, high-gain, low-power, 3.7-dB NF, CMOS LNA fabricated with a 90-nm process. This LNA utilizes a gain-peaking technique to achieve a peak gain of 22 dB and a minimum NF of 3.7 dB while consuming 13.5 mW of power. Fig. 1 shows the design concept and circuit schematic of the proposed 60-GHz high-gain, low-power CMOS LNA.

II. LOW-NOISE AMPLIFIER DESIGN

Conventionally, the cascade stage is widely used for LNAs in a CMOS circuit design, owing to its better isolation and gain performance. In this study, a 2-stage cascade structure with a common-source (CS) buffer amplifier is adopted. The design tradeoffs between power gain and NF are considered for the first two stages. Therefore, the gate-inductive gain-peaking and the inter-stage noise inductor schemes are adopted in the first and second cascade amplifier stages to optimize the maximum available gain and the minimal NF. The tradeoffs between the power gain and linearity are taken for the third stage. The third CS stage with a derivative superposition (DS) technique provides a tuning mechanism to prevent the process-voltage-temperature (PVT) variations.

On the basis of the noise considerations [6], the simulated current density of the 2-stage cascade structure was chosen as 156 μA/μm, and hence nMOS transistors (M1,4) with 16 fingers for the CS stage and the common-gate (CG) stage (each with W/L = 2 μm/0.1 μm per finger) were adopted. In addition, both the gate inductors Lg2 and Lg4 (denoted as TL2 and TL4, respectively) are in a transmission line structure.
A. Inter-stage noise matching inductor

As shown in Fig. 1, the thin-film microstrip (TFMS) line spiral inductors \(L_{m1}\) and \(L_{m2}\) were inserted in series with the signal path between the CS and the CG stages in each cascode structure for noise reduction considerations. The input impedance of the cascode structure from node \(m\), also shown in Fig. 2(a), can be calculated as follows:

\[
Z_m = \frac{V_m}{I_m} = S(L_m + L_s) + \frac{1}{SC_{ds1}} + \frac{g_m1}{C_{ds1}}L_s \tag{1}
\]

Eq. (1) describes the imaginary part of impedance \(Z_m\) that depends on the inter-stage noise matching inductor \(L_m\) and the source degeneration inductor \(L_s\). The imaginary part of impedance \(Z_m\) can eliminate the effects due to parasitic capacitance. Thus, the parasitic resistance of the inductor will cause less noise than the original cascode cell. Fig. 2(b) detects the NF versus different inductances of the \(L_m\) and \(L_s\). It could be seen that the NF is reduced from 4.9 to 3.7 dB at 60 GHz by using the inter-stage noise matching inductor. Furthermore, to achieve a compact size, the TFMS line spiral inductors are designed, which can provide a flexible layout routing. Fig. 2(c) shows the simulated inductance and \(Q\) of the TFMS line spiral inductor \(L_m\). The optimal inductance and \(Q\) value are chosen as 170 \(\text{pH}\) and 16, respectively.

B. Linearity stage

The third CS stage with a DS structure is designed to prevent poor linearity. Generally, the third-order intercept point (IP3) of the \(n\)-stage cascaded system is expressed as follows:

\[
\frac{1}{A_{IP3}} = \frac{1}{A_{IP3,1}^2} + \frac{\alpha_{1}^2}{A_{IP3,2}^2} + \frac{\alpha_{1}^2 \alpha_{p}^2}{A_{IP3,3}^2} + \ldots \tag{2}
\]

Based on eq. (2), the cascode structure provides good isolation, owing to which the third linearity stage will not affect the NF performance. Therefore, noise matching and high linearity performance can be achieved simultaneously.

All the requirements of inter-stage matching are implemented in the conjugate match to achieve maximum power transfer. The matching networks consist of series and shunt transmission lines that are implemented by 50-\(\Omega\) TFMS lines. The TFMS line consists of a bottom metal layer (implemented by M1) serving as the ground plane and a top metal layer (by M9) serving as the microstrip signal line. The width of the TFMS lines is 9 \(\mu\text{m}\), and the line-to-line distance for any pair of TFMS lines is more than three times the line width to avoid any mutual coupling effects. The TFMS line designs are based on the three-dimensional full-wave electromagnetic simulation by Ansoft\textsuperscript{TM} HFSS\textsuperscript{TM}.

III. Measurement Results

The LNA was measured with on-wafer probing. The VDD supply voltage and total current consumption were 1.5 V and 9 mA, respectively. Because the parasitic effects of the RF pads were taken into consideration while performing the simulation, the measured results did not require de-embedding. The measured input return losses (\(S_{11}\)) and output return losses (\(S_{22}\)) from 40 to 67 GHz are plotted in Figs. 3(a) and (b), respectively. From these figures, it is found that both the return losses are well below -10 dB over a frequency range of 57–64 GHz. The related stability \(K\)-factor is greater than 1. Fig. 3(c) shows the measured peak power gain of 22 dB at 57.3 GHz. The simulated and the measured power gain are in good agreement with each other. Fig. 4(a) describes the NF measurement setup. We adopted two RF cables with different lengths (i.e., 60 cm and 120 cm) to verify the measurement (denote as Meas. 1 and Meas. 2). Two noise down-converters are used to cover the measurement frequency from 57 to 64 GHz. Fig. 4(b) shows the measured NF in the desired bandwidth are from 3.7 to 5.2 dB. The average NF is 4.3 dB. Moreover, the gain performances measured by the noise figure analyzer (NFA) are also plotted in Fig. 3(c), which have a good agreement with the PNA’s result. As shown in Fig. 5, the measured input 1-dB compression point (\(P_{1dB}\)) and

![Image](image-url)
Fig. 3  Simulated and measured S-parameters: (a) input return losses ($S_{11}$), (b) output return losses ($S_{22}$), and (c) power gain ($S_{21}$).

Fig. 4  NF measurement: (a) measurement setup and (b) simulated and measured results.

Fig. 5  Simulated and measured results for: (a) input $P_{1dB}$ and (b) input IP3.

Fig. 6  Chip micrograph.

the input IP3 of the amplifier are -23 dBm and -13 dBm at 60 GHz, respectively. Furthermore, Fig. 6 shows the LNA chip micrograph with a size of $0.76 \times 0.78$ mm$^2$. Table I summarizes the performance comparison of our 60-GHz CMOS LNA with the reported LNAs, this work has an impressive NF and FOM performance.

IV. CONCLUSION

This paper presents a 60-GHz, high-gain, low-power, 3.7-dB NF, CMOS LNA fabricated with a 90-nm process. The proposed LNA adopted a two-stage cascode structure with a CS buffer amplifier. The proposed circuit achieves a peak gain of 22 dB at 57.3 GHz with a minimum NF of 3.7 dB; in
### TABLE I

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (CMOS)</th>
<th>Supply Voltage (V)</th>
<th>Topology</th>
<th>Gain (dB)</th>
<th>IIP3 (dBm)</th>
<th>IP1dB (dBm)</th>
<th>NFmin (dB)</th>
<th>Powerdiss (mW)</th>
<th>FOM</th>
</tr>
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<tbody>
<tr>
<td>[7]</td>
<td>0.13 µm</td>
<td>1.5</td>
<td>Current-reused</td>
<td>13.2 @ 58 GHz</td>
<td>-4.7</td>
<td>-15</td>
<td>4.9</td>
<td>29.1</td>
<td>6.8</td>
</tr>
<tr>
<td>[8]</td>
<td>0.13 µm</td>
<td>1.5</td>
<td>3-stage cascode</td>
<td>21 @ 53 GHz</td>
<td>-16</td>
<td>-25</td>
<td>8.3</td>
<td>15.1</td>
<td>1.9</td>
</tr>
<tr>
<td>2011 RFIC [9]</td>
<td>65 nm</td>
<td>1.2</td>
<td>3-stage cascode (with T-Line)</td>
<td>20.6 @ 60 GHz</td>
<td>N/A</td>
<td>-29</td>
<td>4.9 @ 58 GHz</td>
<td>33.6</td>
<td>--</td>
</tr>
<tr>
<td>[10]</td>
<td>65 nm</td>
<td>1.25</td>
<td>3 CS TF + CF</td>
<td>23 @ 60 GHz</td>
<td>-16.5</td>
<td>-26.5</td>
<td>4</td>
<td>8</td>
<td>22.2</td>
</tr>
<tr>
<td>This Work</td>
<td>90 nm</td>
<td>1.5</td>
<td>2-stage cascode + 1 CS</td>
<td>22 @ 57.3 GHz</td>
<td>-13</td>
<td>-23</td>
<td>3.7 @ 61 GHz</td>
<td>13.5</td>
<td>25.4</td>
</tr>
</tbody>
</table>

*FOM = \frac{Gain \times IIP3 \times f}{\text{NF} - 1} \times P_{DC}*

In addition, input IP3 and input IP1dB are -13 dBm and -23 dBm, respectively. Further, the total DC power consumed by the proposed circuit at 1.5 V is 13.5 mW. It should be noted that our proposed LNA has a lower NF, higher gain, and a higher figure of merit (FOM) than the reported state-of-the-art LNAs.

### REFERENCES


