Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD chips

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Introduction

• Digital Microfluidic Biochip (DMFBs)
  
  - Benefits
    ■ High throughput
    ■ High sensitivity
    ■ Low cost
  
  - Applications
    ■ DNA sequencing
    ■ Immunoassays
    ■ Clinical diagnosis
Introduction

• Electrowetting-on-dielectric (EWOD) technique was used to realize DMFBs.
  - 2D microfluidic array: set of basic cells for biological reactions
  - Reservoirs/dispensing ports: for droplet generation
  - Optical detectors: detection of reaction result
  - Droplets: biological sample carrier as basic units to perform the laboratory procedures on a DMFB
Introduction

- Electrowetting-on-dielectric (EWOD) technique was used to realize DMFBs.
  - **2D microfluidic array**: set of basic cells for biological reactions
  - **Reservoirs/dispensing ports**: for droplet generation
  - **Optical detectors**: detection of reaction result
  - **Droplets**: biological sample carrier as basic units to perform the laboratory procedures on a DMFB

![Diagram showing a 2D microfluidic array and droplet system with high voltage to generate an electric field and components like hydrophobic insulation, ground electrode, control electrodes, top plate, and droplet.](Diagram)
Introduction

- Conventional DMFBs
  - Direct addressing for each electrode.

- Pin-constrained issue:
  - As chip size increase, its necessary to limit the number of control pins.

- Broadcast Addressing for pin-constrained problem [Xu et al, DAC’08]
  - Reduce pin count and fabricate cost

![Diagram](a)
```
(a) | e_1 | e_2 |
    | e_3 | e_4 |
    | e_5 | e_6 |
    | e_7 | e_8 |
    | e_9 | e_{10} |
    | e_{11} | e_{12} |
```
```
(c) Pin count: 12
```
```
(d) Pin count: 5
```
Introduction

• Pin-constrained Broadcast Addressing
  - Reduces the pin count by replacing “X” with “1” or “0” to make multiple electrodes share the same control signal.
  - Compatibility is examined among identical and complementary signals.

<table>
<thead>
<tr>
<th>Actuation sequence</th>
<th>e_1</th>
<th>10XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>e_2</td>
<td>010XX</td>
<td></td>
</tr>
<tr>
<td>e_3</td>
<td>XXX11</td>
<td></td>
</tr>
<tr>
<td>e_4</td>
<td>X101X</td>
<td></td>
</tr>
<tr>
<td>e_5</td>
<td>X01XX</td>
<td></td>
</tr>
</tbody>
</table>
Introduction

Pin-constrained Broadcast Addressing

By assigning the same pin for compatible electrode and conduct wire routing, we can obtain a feasible routing solution.

<table>
<thead>
<tr>
<th>Electrode</th>
<th>$e_1$</th>
<th>$e_2$</th>
<th>$e_3$</th>
<th>$e_4$</th>
<th>$e_5$</th>
<th>$e_6$</th>
<th>$e_7$</th>
<th>$e_8$</th>
<th>$e_9$</th>
<th>$e_{10}$</th>
<th>$e_{11}$</th>
<th>$e_{12}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Actuation sequence</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Electrode group</th>
<th>Outcome actuation sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$e_1, e_2$</td>
<td>1 0 0 1 1</td>
</tr>
<tr>
<td>2</td>
<td>$e_{11}, e_{12}$</td>
<td>0 1 1 1 1</td>
</tr>
<tr>
<td>3</td>
<td>$e_6, e_7$</td>
<td>1 0 1 1 1</td>
</tr>
<tr>
<td>4</td>
<td>$e_3, e_4, e_5, e_8$</td>
<td>0 1 0 0 1</td>
</tr>
<tr>
<td>5</td>
<td>$e_9, e_{10}$</td>
<td>1 1 0 1 0</td>
</tr>
</tbody>
</table>
Introduction

- **Main Challenge**: Trapped Charge Problem
Introduction

• Trapped Charge Problem
  – Actuation voltage > Threshold voltage $V_{th}$
    - $V_{th}$ is depended on different materials
    - Different actuation voltage for different operation (ex: 15-40V for transportation)
  – **Drawback**: causing the contact angle saturated thus decrease the reliability.

[1] Shaun Berry, Jakub Kedzierski, and Behrouz Abedian “Irreversible Electrowetting on Thin Fluoropolymer Films,
Introduction

• Trapped Charge Problem
  - Different pin addressing would affect the reliability

<table>
<thead>
<tr>
<th>Electrode</th>
<th>Actuation Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>e₁</td>
<td>XXX01</td>
</tr>
<tr>
<td>e₂</td>
<td>100XX</td>
</tr>
<tr>
<td>e₃</td>
<td>01001</td>
</tr>
</tbody>
</table>

Electrode: e₁ 20V, e₂ 20V, e₃ 80V
• Trapped Charge Problem
  - Assign $e_1$ and $e_3$ the same pin would decrease reliability
Introduction

- This work focuses on the **chip-level design** of the chip.
  - Reliability Pin Assignment
  - Feasible Wire Routing

![Diagram of chip design with labels: Substrate, Electrode, Electrical pads, Conduction wires, Pin, 2D pin array.](image)
Problem Formulation

• Major Constrains
  – Voltage constraint (Threshold Voltage)
  – Broadcast-addressing constraint
  – Pin-count constraint
  – Routing constraint
Problem Formulation

• Input
  – Electrode set: \( E = \{ e_1, e_2, \ldots e_n \} \).
  – Actuation Sequence of each electrode \( e_i \) (ex: “00100”)
  – Required voltage \( V_{ei} \) of each electrode \( e_i \) (ex: dispensing = 100V, routing = 10V, …. )
  – Threshold voltage \( V_{th} \)
  – Pin constraint \( P \)

• Goal
  – Minimize the value of Max \( (V_i^* - V_{ei}) \), \( e_i \in E, V_i^* > V_{th} \)
  – Meet pin constraint and routing constraint

• Output
  – Feasible electrode addressing.
  – Feasible wire routing solution.
Outline

- Introduction
- Problem Formulation
- Algorithms
- Experimental Results
- Conclusion
Algorithm

• Main idea
  – Optimize the reliability while keeping the routability

• The algorithm contains 2 main steps

  Step 1. Incremental Search Method

  Step 2. Simultaneously Broadcast Addressing and Routing
Incremental Search Method

- A value $V_s$ (start from 0) is gradually increasing by 1 for each iteration.
- Under specific $V_s$, build the voltage-constrained compatibility graph ($G_{vcc}$).
  - An edge was constructed between two electrode a, b iff
    1. $V_{max_{ab}} - \max(V_{th}, V_{da}) \leq V_{bound}$
    2. $V_{max_{ab}} - \max(V_{th}, V_{db}) \leq V_{bound}$

![Diagram of electrode connections with voltages and constraints]
Incremental Search Method

- If we can find a routing solution under $V_s$, then we can obtain a feasible solution with $V_{d\text{max}} \leq V_s$

- Try to obtain a feasible routing solution based on $G_{vcc}$

(a) Original $G_c$

(b) $G_{vcc}$ with $V_s = 30$

(c) $G_{vcc}$ with $V_s = 10$
Simultaneously Broadcast Addressing And Routing

- Pin Merge
  - Merge **addressed pins** to **unaddressed electrodes** by MCMF
  - Wire routing are conducted after pin merge.
Simultaneously Broadcast Addressing And Routing

- **Min-cost Maximum-flow (MCMF) formulation**
  - The cost of edges are set to HPWL-Extension

![Diagram of network with nodes and edges representing existed pins and unaddressed electrodes, with capacity and cost annotations.](image)

**HPWL Extension = 6**
Simultaneously Broadcast Addressing And Routing

• Wire Routing
  - For each net in the result of addressing, we start to route them by breadth-first-search (BFS) based algorithm.
  - A fail route occurs when:
    ▪ (1) No routing path exist – drop this addressing solution.
    ▪ (2) Some electrode which is blocked by other electrode. Increase the cost of previous path and reroute again.
5 real-life chip were used for test cases.

<table>
<thead>
<tr>
<th>Chip</th>
<th>Size</th>
<th>#E</th>
<th>$P_{\text{max}}$</th>
<th>Avg. $V_{\text{pre}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>amino</td>
<td>6 X 8</td>
<td>20</td>
<td>16</td>
<td>32.8</td>
</tr>
<tr>
<td>Multiplex</td>
<td>15 X 15</td>
<td>59</td>
<td>32</td>
<td>17.5</td>
</tr>
<tr>
<td>PCR</td>
<td>15 X 15</td>
<td>62</td>
<td>32</td>
<td>21.9</td>
</tr>
<tr>
<td>Multifunctional</td>
<td>15 X 15</td>
<td>91</td>
<td>64</td>
<td>19.7</td>
</tr>
<tr>
<td>DNA preparation</td>
<td>13 X 21</td>
<td>77</td>
<td>32</td>
<td>20.8</td>
</tr>
</tbody>
</table>
Experimental Result

- Result Table
  - Compared to [10], we obtained low $V_{d_{\text{max}}}$ and successful wire routing in all test cases.

### TABLE II: ELECTRODE ADDRESSING COMPARISON BETWEEN [10] AND OURS

<table>
<thead>
<tr>
<th>Chip</th>
<th>[10]</th>
<th>Ours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{d_{\text{max}}}$</td>
<td>$V_{d_{\text{max}}}$</td>
</tr>
<tr>
<td>amino</td>
<td>57</td>
<td>2</td>
</tr>
<tr>
<td>multiplex</td>
<td>56</td>
<td>24</td>
</tr>
<tr>
<td>PCR</td>
<td>54</td>
<td>40</td>
</tr>
<tr>
<td>multifunctional</td>
<td>55</td>
<td>40</td>
</tr>
<tr>
<td>DNA preparation</td>
<td>57</td>
<td>19</td>
</tr>
<tr>
<td>Total</td>
<td>128</td>
<td></td>
</tr>
</tbody>
</table>

### TABLE III: WIRE ROUTING COMPARISON BETWEEN [10] AND OURS

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#Pin</td>
<td>WL</td>
</tr>
<tr>
<td>amino</td>
<td>13</td>
<td>206</td>
</tr>
<tr>
<td>multiplex</td>
<td>7</td>
<td>N/A</td>
</tr>
<tr>
<td>PCR</td>
<td>12</td>
<td>N/A</td>
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<tr>
<td>DNA preparation</td>
<td>22</td>
<td>N/A</td>
</tr>
<tr>
<td>Total</td>
<td>132</td>
<td></td>
</tr>
</tbody>
</table>
Experimental Result

- The comparison of voltage difference ($V_d$) distributions for all test cases. ([10] vs. Ours)

Experimental Result

- Result of **multifunctional assay**
- Size: 15x15
- #Electrode: 91
- Pin Constraint: 64
- #Pin: 64
- $V_{dmax} : 0$
Conclusion

• We presented electrode addressing and wire routing algorithm for voltage-aware, reliability-driven pin-constrained EWOD chips.

• The experimental results on a set of real-life applications demonstrated that the proposed approach was very effective and efficient.
• Q & A
Thank You!