Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips

Abstract (論文摘要)

Electrowetting-on-dielectric (EWOD) chips have become the most promising technology to realize pin-constrained digital microfluidic biochips (PDMFBs). In the design flow of EWOD chips, reliability is a critical challenge as it directly affects execution of bioassays. The major factor to degrade chip reliability is the trapped charge problem, which is induced by excessive applied voltage. Nevertheless, to comply with the pin constraint for PDMFBs, signal merging is inevitably involved, and thereby incurring trapped charges due to unawareness of applied voltage. Except for the trapped charge problem, wire routing to accomplish electrical connections increases the design complexity of pin-constrained EWOD chips. Unfortunately, no existing works tackle the problems of excessive applied voltage and wire routing, and thus the resultant chip will have more probabilities to fail during execution or can not be realized because of wire routing problem. In this paper, we present a network-flow based algorithm for reliability-driven pin-constrained EWOD chips with the consideration of voltage issue. Our algorithm not only minimizes the reliability problem induced by signal merging but also provides a comprehensive routing solution for EWOD chip-level designs. The experimental results demonstrate the effectiveness of proposed algorithm on real-life chips.