Novel Isolated High-step-up DC–DC Converter with Voltage Lift

Tsorng-Juu Liang, Member, IEEE, Jian-Hsieng Lee, Shih-Ming Chen, Jiann-Fuh Chen, Member, IEEE, and Lung-Sheng Yang

Abstract — A novel two-switch high-step-up isolated converter with voltage lift is proposed in this paper. The proposed isolated converter utilizes a transformer with low turn ratio to achieve high step-up gain. The secondary winding charges two boosting capacitors in parallel as switches during the switch-on period, and two boosting capacitors are discharged in series during switch-off period. Thus, the converter has high voltage gain with appropriate duty ratio. In addition, by using two clamping diodes and capacitor on the primary side, leakage energy is recycled and the voltage spikes of the two active switches are clamped, thereby improving conversion efficiency. Finally, experimental results based on a prototype implemented in the laboratory with input voltage 24 V, output voltage 200 V, and output power 200 W verify the performance of the proposed isolated converter; full-load efficiency is nearly 93%.

Index Terms — High-step-up, two-switch isolated converter, voltage lift technique, high voltage gain

I. INTRODUCTION

In 2011, the March 11 earthquake in Japan severely damaged several reactors at the Fukushima Nuclear Plant, thereby releasing a significant amount of radioactive material into the atmosphere. This event has led people to consider global abolishment of nuclear power plant operations. Furthermore, in recent years, massive amounts of petrochemical energy has been used, producing high levels of pollution that cause drastic climate change from the release of greenhouse gases. Thus, the development of clean and green renewable energy conversion systems, such as photovoltaic (PV), fuel cell, and tide energy conversion systems need to be accelerated. Front-end stage circuits of these applications need a high-step-up converters. These converter can be also applied in battery backup systems for uninterrupted power supplies (UPS) and high-intensity discharge (HID) lamp ballasts for motorcycle/automobile lighting also require high-step-up converters [1],[2].

Conventional isolated converters such as flyback, forward, push–pull, and SEPIC converters can achieve high voltage gain by adjusting the turn ratio of the transformer. However, leakage of inductance energy in the transformer causes high voltage spikes in the switches, reducing system efficiency [3]–[5]. In order to reduce the voltage spike, snubber circuits can be used to reduce the voltage spike, such as resistor–capacitor–diode (RCD) snubber circuits, non-dissipative snubber circuits, and active clamp circuits [7]–[9].

Many non-isolated topologies have been presented to obtain high step-up voltage gain in the past decade [10]–[26]. These non-isolated converters can be used with the coupled-inductor [10]–[16], cascaded technique [17]–[22], and switched-inductor and switched-capacitor techniques [23]–[26] to obtain high voltage gain with the appropriate duty ratio. However, non-isolated converters cannot meet the safety standards needed in galvanic isolation. In order to meet the safety standards of galvanic isolation, some isolated converters for high-step-up applications have been proposed. These converters are secondary-series boost converters [27],[28], voltage-lift techniques [29],[30], and boost-type converters integrated with transformer [31],[32] to obtain high voltage gain. Active clamp circuits can be used to recycle energy leakage and also reduce voltage spike of switches. Since these circuits require two or more drive signals. This will increase the drive circuit and control complexity.

This paper proposes a novel high-efficiency high-step-up isolated DC–DC converter using one control gate driver signal and diodes $D_1$ and $D_2$ to recycle leakage energy of the transformer to the input side. According to the concept of charge in parallel and discharge in series, output capacitors $C_1$ and $C_2$ and diode $D_1$ and $D_2$ are utilized to form two voltage double circuits and obtain high voltage gain. The system configuration of the proposed isolated DC–DC topology is depicted in Fig. 1. The circuit includes DC input voltage $V_{in}$, input capacitor $C_{in}$, two clamping diodes $D_1$ and $D_2$, two active switches $S_1$ and $S_2$, transformer $T_r$, two boosting capacitors $C_1$ and $C_2$, two boosting diodes $D_1$ and $D_2$, output diode $D_o$, output capacitor $C_{out}$, output load $R$. Switches $S_1$ and $S_2$ are controlled simultaneously by one control signal. The transformer includes magnetizing inductance $L_m$ and leakage inductance $L_{lp}$ and $L_{lp}$. Compared with the flyback converter or other high-step up isolated converters [29],[30] in the same output voltage, the transformer only needs a small safety standard distance.

The features of proposed isolated converter are as follows: 1) meets the safety standards of galvanic isolation.
II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

In order to simplify the analysis of the proposed converter, the following are assumed over one switching period:

1) The capacitors \( C_{in}, C_1, C_2, \) and \( C_3 \) are large enough; thus, \( V_{in}, V_{C1}, V_{C2}, \) and \( V_o \) are regarded as constant values.
2) The active switches and all diodes are regarded as ideal.
3) The turn ratio of the transformer is defined as

\[
 n = \frac{N_s}{N_p}
\]  

(1)

where \( N_p \) and \( N_s \) are the winding turns in the primary and secondary side, respectively.

4) The parasitic inductors, capacitors, and resistors of circuit traces are ignored.

(A) CCM Operation

The key waveforms of the proposed converter at continuous condition mode (CCM) operation is depicted in Fig. 2 and discussed in detail below. In CCM operation, the operating mode of the proposed isolated converter can be divided into six operating modes over one switching period:

1) Mode I \([t_0, t_1]\): During this subinterval, active switches \( S_1 \) and \( S_2 \) are simultaneously on. Diodes \( D_1, D_2, D_3, \) and \( D_4 \) are reverse-biased, whereas \( D_5 \) is forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(a). The primary magnetizing inductance \( L_m \) stores energy from the DC input voltage \( V_{in} \). The voltage across magnetizing inductance \( L_m \) and leakage inductance \( L_k \) in series is \( V_{in} \). The primary current of \( i_{in}, i_{Lm}, i_{LK}, \) and \( i_{swap} \) are equal. The current continuously increases. However, the secondary winding current \( i_s \) decreases because the secondary leakage inductor \( L_k \) limits the flow to the output. The secondary winding voltage \( V_{Ls} \) and boosting voltages \( V_{C1} \) and \( V_{C2} \) are linked in series to release energy to the output capacitor \( C_o \) and the output load \( R \). When secondary winding current \( i_s \) drops to zero, boosting capacitors \( C_1 \) and \( C_2 \) begin to charge the DC input voltage \( V_{in} \). The energy is delivered from the primary side \( N_p \) to secondary side \( N_s \) through \( D_3 \) and \( D_4 \). This operating mode ends when \( i_{Lk} = i_{D2} \) at \( t = t_1 \).

2) Mode II \([t_1, t_2]\): During this subinterval, switches \( S_1 \) and \( S_2 \) remain simultaneously on. Diodes \( D_1, D_2, \) and \( D_4 \) are reverse-biased, whereas \( D_3 \) and \( D_5 \) are forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(b). The primary magnetizing inductance \( L_m \) continues to store energy from the DC input voltage \( V_{in} \). Portions of the energy from DC input voltage \( V_{in} \) is delivered to the secondary winding through \( D_3 \) and \( D_4 \) to charge the boosting capacitors \( C_1 \) and \( C_2 \), respectively. The voltages across \( C_1 \) and \( C_2 \) are nearly equal to \( nV_{in} \), whereas the current \( i_{D1} \) is almost equal to \( i_{D2} \). The output capacitor \( C_o \) is released energy to output load \( R \). This operating mode ends when active switches \( S_1 \) and \( S_2 \) are turned off simultaneously at \( t = t_2 \).

3) Mode III \([t_2, t_3]\): During this subinterval, active switches \( S_1 \) and \( S_2 \) are simultaneously off. Diodes \( D_1, D_2, \) and \( D_4 \) are reverse-biased, whereas \( D_3 \) and \( D_5 \) are forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(c). The leakage current \( i_{Lk} \) charges the parasitic capacitor \( C_{DS1} \) and \( C_{DS2} \) of active switches \( S_1 \) and \( S_2 \). The voltages of \( V_{S1} \) and \( V_{S2} \) increase until \( t_3 \). Boosting capacitors \( C_1 \) and \( C_2 \) continue to charge the DC input voltage \( V_{in} \) through the secondary winding. \( D_3, D_5 \), and output capacitor \( C_o \) continue to release energy to output load \( R \). This operating mode ends when the voltage \( V_{S1} \) and \( V_{S2} \) are equal to \( V_{in} \); diodes \( D_1, D_2, \) and \( D_4 \) are forward-biased at \( t = t_3 \).

4) Mode IV \([t_3, t_4]\): During this subinterval, active switches \( S_1 \) and \( S_2 \) are simultaneously turned off. Diodes \( D_1, D_2, D_3, \) and \( D_5 \) are forward-biased, whereas \( D_5 \) is reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(d). The leakage current \( i_{Lk} \) flows through \( D_3 \) and \( D_5 \) to charge the input capacitor, clamping the maximum spike voltage of the two active switches so that the leakage energy can be recycled. The leakage current \( i_{Lk} \) decreases quickly. Boosting capacitors \( C_1 \) and \( C_2 \) continue to produce energy in parallel mode. This operating mode ends when the clamping diode currents \( i_{D1} \) and \( i_{D2} \) equal zero at \( t = t_4 \).

5) Mode V \([t_4, t_5]\): During this subinterval, active switches \( S_1 \) and \( S_2 \) are simultaneously off. Diode \( D_6 \) is forward-biased, whereas diodes \( D_1, D_2, D_3, \) and \( D_4 \) are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(e). The two capacitors \( C_{DS1} \) and \( C_{DS2} \) voltage decays are caused by resonant current through the leakage inductance \( L_k \) and the parasitic capacitor \( C_{DS1} \) and \( C_{DS2} \) of active switches \( S_1 \) and \( S_2 \). Boosting capacitors \( C_1 \) and \( C_2 \) still produce energy in parallel mode and output capacitor \( C_o \) continues to release energy to output load \( R \). This operating mode ends when capacitors \( C_{DS1} \) and \( C_{DS2} \) are equal to \( (V_{o}/R - V_{in})/2 \) at \( t = t_5 \).

6) Mode VI \([t_5, t_6]\): During this subinterval, active switches \( S_1 \) and \( S_2 \) are simultaneously off. Diode \( D_6 \) is forward-biased,
whereas diodes \( D_1, D_2, D_3, \) and \( D_4 \) are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(f). The energy of magnetizing inductance \( L_m \) is delivered to the secondary winding \( N_p \) and \( N_s \). Secondary-side voltage \( V_L \) is linked in series with \( V_{C1} \) and \( V_{C2} \) to release energy to output capacitor \( C_o \) and output load \( R \). This operating mode ends when active switches \( S_1 \) and \( S_2 \) are turned on simultaneously at \( t = t_o \).

![Fig. 2. Key waveforms of the proposed converter at CCM operation](image-url)
(f) Mode VI

Fig. 3. Equivalent circuits of the isolated DC–DC converter over one switching period at CCM operation: (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV; (e) Mode V; (f) Mode VI.

(B) DCM Operation

The key waveforms of the proposed converter at discontinuous condition mode (DCM) operation is depicted in Fig. 4. To simplify the analysis for DCM operation mode, the leakage inductances $L_{kp}$ and $L_{ks}$ of the transformer are neglected. Equivalent circuits of the isolated DC–DC converter over one switching period at DCM operation are depicted in Fig. 5. There are three operating modes in DCM:

1) Mode I [$t_0, t_1$]: During this sub-interval, active switches $S_1$ and $S_2$ are simultaneously on. Diodes $D_1$, $D_2$, and $D_0$ are reverse-biased, whereas $D_3$ and $D_4$ are forward-biased. The equivalent circuit of the isolated DC-DC converter is depicted in Fig. 5(a). The primary magnetizing inductance $L_m$ stores energy from the DC input voltage $V_{in}$. Portions of the energy by DC input voltage $V_{in}$ is delivered to the secondary winding through $D_3$ and $D_4$ to charge capacitors $C_1$ and $C_2$. The voltages across $C_1$ and $C_2$ are nearly equal to $nV_{in}$, and current $i_{D3}$ is nearly equal to $i_{D4}$. Output capacitor $C_o$ releases energy to output load $R$. This operating mode ends when active switches $S_1$ and $S_2$ are turned off at $t = t_1$.

2) Mode II [$t_1, t_2$]: During this subinterval, active switches $S_1$ and $S_2$ are simultaneously off. Diode $D_0$ is forward-biased, whereas diodes $D_1$, $D_2$, $D_3$, and $D_4$ are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 6(b). The magnetic energy of $L_m$, $C_1$, and $C_2$ are released to output capacitor $C_o$ and output load $R$. This mode ends when the energy stored in $L_m$ is depleted at $t = t_2$.

3) Mode III [$t_2, t_3$]: During this subinterval, active switches $S_1$ and $S_2$ are simultaneously off. Diodes $D_1$, $D_2$, $D_3$, $D_4$, and $D_0$ are reverse-biased. The equivalent circuit of the isolated DC-DC converter is depicted in Fig. 6(c). The energy stored in output capacitor $C_o$ is discharged to load $R$. This mode ends when active switches $S_1$ and $S_2$ are turned on at $t = t_3$. 

![Fig. 4. Key waveforms of the proposed converter at DCM operation](image-url)
III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

In steady-state condition analysis, total leakage inductance of the proposed isolated converter continues to be ignored.

(A) CCM Operation

While active switches $S_1$ and $S_2$ are simultaneously on, $D_3$ and $D_4$ are forward-biased. The primary magnetizing inductance voltage $v_{Lp}$, boosting capacitors voltage $C_1$ and $C_2$ are given by

$$v_{Lp} = V_n$$
$$v_{C1} = v_{C2} = nV_n$$

While active switches $S_1$ and $S_2$ are simultaneously off, the primary magnetizing-inductance voltage $v_{Lp}$ for this interval is

$$v_{Lp} = 2V_n - \frac{V_o}{n}$$

Application of the principle of volt-second balance to primary-side magnetizing inductance $L_m$ yields

$$\int_{0}^{T_s} V_n dt + \int_{0}^{T_s} (2V_n - \frac{V_o}{n}) dt = 0$$

Using (5), the voltage gain is

$$M_{CCM} = \frac{V}{V_n} = \frac{n(2-D)}{1-D}$$

(B) DCM Operation

In DCM operation, three modes are discussed. The key waveform is depicted in Fig. 4.

When active switches $S_1$ and $S_2$ are simultaneously on, $D_3$ and $D_4$ are forward-biased. The primary magnetizing-inductance voltage $v_{Lp}$, capacitors voltage $C_1$ and $C_2$ are given by

$$v_{Lp} = V_n$$
$$v_{C1} = v_{C2} = nV_n$$

The peak value of the magnetizing inductance current is given by

$$I_{Lmp} = \frac{V_n}{L_m} D T_s$$

When active switches $S_1$ and $S_2$ are simultaneously off, the primary magnetizing-inductance voltage $v_{Lp}$ for this interval is

$$v_{Lp} = 2V_n - \frac{V_o}{n}$$

The peak value of the magnetizing inductance current is given by

$$I_{Lmp} = \frac{V_n}{L_m} 2 T_s$$

Based on (6), the voltage gain compared of traditional flyback converter and proposed converter at CCM operation with turn ratio $n=3$ is depicted in Fig. 6. From Fig. 6, the voltage gain of the proposed converter becomes higher than the traditional flyback converters.
When active switches $S_1$ and $S_2$ are simultaneously off, output diode $D_{o}$ is reverse-biased. The primary magnetizing inductance voltage $v_{Lp}$ for this interval is

$$v_{Lp} = 0$$  \hspace{1cm} (16)

Application of the principle of volt-second balance to primary-side magnetizing inductance $L_m$ yields

$$\int_{0}^{\tau} V_{o} \, dt + \int_{n \cdot \tau}^{(n+1) \cdot \tau} (2V_{o} - \frac{V_{n}}{n}) \, dt + \int_{(n+1) \cdot \tau}^{\tau} 0 \, dt = 0$$  \hspace{1cm} (17)

Using (17), the duty cycle $D_2$ is given by

$$D_2 = \frac{V_o D_1}{V_o - 2V_n}$$

Based on Fig. 4, the average current of $i_C$ is obtained as

$$I_{C} = \frac{1}{2n} D_2 I_{mp} - I_O$$  \hspace{1cm} (19)

Substituting (13), (18), and $I_C = 0$ into Equation (19) yields

$$I_{o} = \frac{1}{2nL_m} \left( \frac{V_o D_1 \tau_s}{V_o - 2V_n} \right) - \frac{V_o}{R}$$

Because $I_C$ equals zero under steady state, (20) can be rewritten as

$$\frac{1}{2nL_m} \left( \frac{V_o D_1 \tau_s}{V_o - 2V_n} \right) = \frac{V_o}{R}$$

The normalized magnetizing inductance time constant is defined as

$$\tau \equiv \frac{L_m}{RT_s}$$  \hspace{1cm} (22)

where $T_s$ is the switching period.

Substituting (22) into (21), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_n} = n + \sqrt{n^2 + \frac{D_1^2}{2\tau}}$$  \hspace{1cm} (23)

(i.e., voltage gain versus duty ratio at DCM operation with different $\tau$ and at CCM operation under $n = 3$).

Using (23), the voltage gain versus duty cycle at CCM and DCM with different $\tau$ is depicted in Fig. 7.

(C) Boundary Operating Condition between CCM and DCM

If the proposed converter is operated in boundary-condition mode (BCM) (Figs. 2 and 4), the output current of BCM $I_{ob}$ is given by

$$I_{ob} = \frac{V_o}{R} = \frac{D}{2L_m} \left( \frac{1}{n} \right) \left( 1 - D \right)^2 T_s$$  \hspace{1cm} (25)

The boundary normalized magnetizing inductance time constant defined as

$$\tau_{LB} \equiv \frac{L_m}{RT_S}$$  \hspace{1cm} (26)

Using (25), $\tau_{LB}$ can be obtained as

$$\tau_{LB} = \frac{D(1 - D)^2}{2n^2(2 - D)}$$  \hspace{1cm} (27)

The curve of $\tau$ is plotted in Fig. 8. If $\tau$ is smaller than $\tau_{LB}$, the proposed isolated converter is operated in DCM; otherwise, the proposed isolated converter is operated in CCM.
IV. DESIGN AND EXPERIMENT OF THE PROPOSED CONVERTER

The laboratory prototype sample is implemented to demonstrate the practicability of the proposed isolated converter. The system specifications and components are as follows:

1) Input DC voltage $V_{\text{in}}$: 24 V
2) Output DC voltage $V_o$: 200 V
3) Maximum output power: 200 W
4) Operating frequency: 50 kHz
5) Input capacitor $C_{\text{in}}$: 3300 $\mu$F/35 V aluminum capacitor
6) Diodes $D_1$ and $D_2$: SBR20A60CTFP Schottky diode
7) Switches $S_1$ and $S_2$: IRLB3036
8) Transformer: ETD-59, core PC-40, $N_p:N_s = 1:3$, $L_m = 43.5$ $\mu$H; $L_k = 0.27$ $\mu$H
9) Boosting capacitors $C_1$ and $C_2$: 100 $\mu$F/ 250 V aluminum capacitor
10) Diodes $D_3$, $D_4$, and $D_0$: MBR20200CT Schottky diode
11) Output capacitor $C_o$: 220 $\mu$F/ 250 V aluminum capacitor

The experimental results at full load $P_o = 200$ W and $V_{\text{in}} = 24$ V are shown in Fig. 9. Figure 9(a) shows the waveforms $v_{S1}$, $v_{S2}$, $i_{D1}$, and $i_{D2}$. The current waveform $i_{D1}$ equals $i_{D2}$ because their current path is the same. In addition, $i_{D1}$ and $i_{D2}$ indicate that the leakage energy is recycled when $S_1$ and $S_2$ are turned off. The reduced loss is approximated 3.4 W. Figure 9(b) shows the waveforms of $v_{D1}$, $v_{D2}$, and $i_{Lk}$. Figure 9(c) shows the waveforms of $v_{C1}$, $v_{C2}$, $i_{D3}$, and $i_{D4}$. Capacitors $C_2$ and $C_3$ are similar to forward converters charging energy in parallel when switches $S_1$ and $S_2$ are turned on, and the discharged energy in series is similar to a flyback converter when switches $S_1$ and $S_2$ are turned off. Current $i_{D3}$ is approximately equal to $i_{D4}$. Figure 9(d) shows the waveforms of $v_{D3}$, $v_{D4}$, and $i_{S}$. The voltage stresses of $D_1$ and $D_2$ are approximately equal. The current of secondary winding $i_S$ is equal to $i_{D3} + i_{D4}$ when switches $S_1$ and $S_2$ are turned on. Figure 9(e) shows the voltage and current waveforms of $v_{Do}$ and $i_{Do}$. The experimental results at $P_o = 40$ W and $V_{\text{in}} = 24$ V are shown in Fig. 10. The voltage waveforms of $v_{S1}$, $v_{S2}$, $v_{D1}$, $v_{D2}$, $v_{D3}$, and $v_{D4}$ have some oscillations caused by the parasitic capacitors $C_{D1}$ and $C_{D2}$ of the active switches $S_1$ and $S_2$. The primary magnetizing inductance $L_m$ and the leakage inductance $L_k$ are formed in resonance when $i_{Lk} = 0$. Figure 11 shows the experimental conversion efficiency of the proposed isolated converter. Maximum efficiency is 96.2%, and efficiency is 92.9% at full load. High current on primary side cause higher conduction loss and resistance $R_T$ of transformer loss under high power condition. Thus, the efficiency is decreased at high power. Hence, the efficiency decays when the output power increases. The power loss analysis of the proposed converter at full load $P_o = 200$ W and $V_{\text{in}} = 24$ V are shown in Table 1 [33],[34]. The measured efficiency at 92.9 % and the calculated results at 95.52 % are slightly different, because the calculated results are losses of neglect switching, iron, and resistance of circuit traces.
Fig. 9. Experimental waveforms at $P_o = 200$ W

Fig. 10. Experimental waveforms at $P_o = 40$ W

Fig. 11. Experimental conversion efficiency of proposed isolated converter

Table 1. Power loss analysis of the proposed converter at full load 200W

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
<th>Loss (W)</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switches $S_1$ and $S_2$</td>
<td>1.9 mΩ</td>
<td>0.58</td>
<td>0.29</td>
</tr>
<tr>
<td>Clamping Diodes $D_1$ and $D_2$</td>
<td>0.7 V</td>
<td>0.2</td>
<td>0.1</td>
</tr>
<tr>
<td>Resistance $R_T$ of transformer</td>
<td>28 mΩ</td>
<td>5.24</td>
<td>2.62</td>
</tr>
<tr>
<td>Boosting diode $D_3$ and $D_4$</td>
<td>0.7 V</td>
<td>2.8</td>
<td>1.4</td>
</tr>
<tr>
<td>Output diode $D_0$</td>
<td>0.7 V</td>
<td>0.7</td>
<td>0.35</td>
</tr>
<tr>
<td><strong>Total loss</strong></td>
<td></td>
<td><strong>9.52</strong></td>
<td><strong>4.76</strong></td>
</tr>
</tbody>
</table>
In this paper, forward and flyback converters are successfully integrated using voltage-lift technique to achieve high voltage gain. Energy stored in the primary leakage inductance during on-time is returned to \( V_a \) via clamping diodes \( D_1 \) and \( D_2 \). This not only improves converter efficiency, it also reduces voltage spike of active switches such that low-voltage stresses and low on-resistance \( R_m \) switches can be selected. The CCM and DCM operating principle and steady state of voltage gain are analyzed in detail. Finally, a prototype of the proposed converter with input voltage 24 V, output voltage 200 V, output power 200 W, maximum efficiency of 96.2\%, and switch voltage spikes lower than 48 V is achieved in the laboratory.

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