Multiple-input multiple-output (MIMO) techniques have been widely used in various wireless communication systems these days. QR factorization is a fundamental module yet computationally intensive used in many MIMO detection schemes. In this paper, a complex-valued QR factorization (CQRF) scheme realized via a sequence of real-value Givens rotations is first presented. An efficient CQRF design using coordinate rotation digital computer (CORDIC) modules is next developed. The design features a highly parallel architecture to support high throughput operations. One CQRF can be obtained in every 8 clock cycles. To reduce the circuit complexity, a pipelined CORDIC structure is also applied. The implementation results in TSMC 0.18-um CMOS process indicate that the proposed design can achieve a throughput rate of 25M CQRFs per second while consuming only 103.7k gates in circuit complexity. Performance evaluation based on a composite index consisting of area and throughput rate also shows the advantages of the proposed design against other similar works.