Novel High Step-Up DC-DC Converter with Coupled-Inductor and Switched-Capacitor Technique for Sustainable Energy System

Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang
Department of Electrical Engineering, National Cheng Kung University, Taiwan

Abstract—In this paper, a novel high step-up DC-DC converter is proposed for sustainable energy system. The proposed converter uses coupled inductor and switched-capacitor technique. The capacitors are charged in parallel and are discharged in series by the coupled-inductor to achieve high step-up voltage gain with appropriate duty ratio. Besides, the voltage stress on the main switch are reduced with a passive clamp circuit, low ON-state resistance $R_{DS(ON)}$ of the main switch can be adopted to reduce the conduction loss. In addition, the reverse-recovery problem of the diode is alleviated by coupled inductor. Thus, the efficiency can be further improved. The operating principle and steady-state analyses of voltage gain are discussed in detail. Finally, a prototype circuit with 24-V input voltage, 400-V output voltage, and 200-W output power is implemented in the laboratory to verify the performance of the proposed converter.

Index Terms—High step-up voltage gain, sustainable energy system, coupled inductor, switched capacitor

I. INTRODUCTION

High step-up DC-DC converters are now widely used in many applications. For example, photovoltaic arrays in sustainable energy system which are the source with low-voltage, the DC-DC converter needs to boost low voltage to high voltage for generating AC utility voltage [1]-[3]. Thus, the high step-up DC-DC converter needs high voltage gain, high efficiency, and small volume [4]-[6]. Theoretically, conventional boost converter can be adopted to provide high step-up voltage gain with extremely high duty ratio. In practice, the step-up voltage gain is limited by the effect of power switch, rectifier diode, and equivalent series resistance (ESR) of inductor and capacitor. Also, the extreme high duty-ratio operation may result in serious reverse-recovery problem, low efficiency and the electromagnetic interference (EMI) problem [7]-[9]. Some converters such as flyback, forward, push-pull, half-bridge, and full-bridge can adjust the turns ratio of a transformer to achieve high step-up voltage gain. However, the main switch of these converters will suffer high voltage spike and high power dissipation caused by the leakage inductor of the transformer [10]. To improve these drawbacks, a non-dissipative snubber circuit and an active-clamp circuit are used. However, the cost will be increased due to the extra power switch and high side driver [11].

Many topologies have been proposed to improve conversion efficiency and achieve high step-up voltage gain [12]-[33]. High step-up gain can be achieved by a switched-capacitor or voltage-lift technique [12]-[18]. However, the main switch suffers high transient current, the conduction loss is increased. The converters with the coupled-inductor technique can achieve high step-up gain by adjusting the turns ratio [19], [20]. However, the leakage inductor issue that relates to the voltage spike on the main switch and the conversion efficiency is important. For this reason, the converters using a coupled inductor with an active clamp circuit have been proposed [21], [22]. Also, an integrated boost-flyback converter is presented. The secondary side of the coupled-inductor is used as a flyback type to achieve high step-up gain [23], [24]. The energy of leakage inductor is recycled into the output during the switch-off period. Thus, the voltage spike of the main switch is limited. Additionally, the voltage stress of the main switch can adjust through the turns ratio of the coupled-inductor. To achieve large high step-up gain, the converter used the secondary side of the coupled-inductor used as a flyback and a forward type has been proposed [25]-[27]. Also, many converters using the coupled-inductor technique are proposed to achieve high step-up gain. Several converters that combine the output-voltage stacking to increase voltage gain are proposed [28]-[30]. The boost-sepic converter with the coupled-inductor and output stacking techniques has been proposed [31]. The high step-up boost converters that use multiple coupled-inductor of output stacking are proposed [32], [33]. The converters with the coupled-inductor technique increase the voltage gain by adding the number of turns ratio and extra additional winding stages.

To achieve high voltage gain and high efficiency, this paper proposes a novel high step-up voltage gain converter. The proposed converter uses the coupled-inductor and switched-capacitor techniques to achieve high step-up voltage gain. The coupled-inductor is operated as the flyback and forward converters. Thus, the capacitors can charge in parallel and discharge in series by secondary-side of the coupled-
inductor. Besides, the secondary-side leakage inductor of the coupled inductor can alleviate the reverse-recovery problem of diodes, the loss can be reduced. However, the leakage inductor of the coupled-inductor may cause high power loss and high voltage spike. Thus, a passive clamping circuit is needed to recycle the energy of the leakage inductor and to clamp the voltage level of the main switch.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit topology of the proposed converter, which is composed of a boost converter with the coupled inductor and switched capacitors. The equivalent circuit model of the coupled inductor includes the magnetizing inductor $L_m$, leakage inductor $L_k$ and an ideal transformer. This converter consists of one power switch, six diodes and six capacitors. The leakage-inductor energy of the coupled inductor is recycled to capacitor $C_1$, and thus the voltage across the switch $S$ can be clamped. Also, the voltages across capacitors $C_2$, $C_3$, $C_4$ and $C_5$ can be adjusted by the turns ratio of the coupled inductor. For this reason, the voltage level of the switch is reduced significantly and low conducting resistance $R_{con}$ of the switch can be used. Thus, the efficiency of the proposed converter can be increased and high step-up voltage gain can be achieved.

To simplify the circuit analysis, the following conditions are assumed:

1) Capacitors $C_1$-$C_5$ and $C_o$ are large enough. Thus, $V_{c1}$, $V_{c4}$ and $V_o$ are considered as constant in one switching period.

2) The power devices are ideal, but the parasitic capacitor of the power switch is considered.

3) The coupling-coefficient of the coupled-inductor $k$ is equal to $L_m/(L_m+L_k)$ and the turns ratio of the coupled-inductor $n$ is equal to $N_s/N_p$.

The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analyzed as follows.

(A) CCM Operation

Based on the above assumptions, there are five operating modes discussed in one switching period under CCM operation. Fig. 2 illustrates the typical waveforms and Fig. 3 shows the topological stages of the proposed converter. The operating modes are described as follows:

1) Mode I [$t_o$, $t_1$]: During this time interval, $S$ is turned on to initiate this mode. Diodes $D_1$, $D_2$, and $D_3$ are reverse biased, and $D_4$, $D_5$ and $D_o$ are forward biased. The current-flow path is shown in Fig. 3(a). The primary current of $i_{L_k}$ increases linearly. The magnetizing inductor $L_m$ begins to store the energy from DC-source $V_{in}$. Due to leakage inductor $L_k$, the secondary-side current $i_s$ decreases linearly. Secondary-side voltage $V_{c2}$, $V_{c3}$ and $V_{c5}$ are connected in series to charge the high-voltage output capacitor $C_2$, and to provide the energy to load $R$. Also, the leakage-inductor energy is recycled to capacitors $C_3$ and $C_4$. Because of the leakage inductor of the coupled inductor, the reverse-recovery problem of the diode is alleviated. When current $i_s$ becomes zero, the energy of DC-source $V_{in}$ is transferred to capacitors $C_2$ and $C_3$ via the coupled inductor. Until the current $i_{Do}$ is equal to zero at $t = t_1$, this operating mode is ended.

2) Mode II [$t_1$, $t_2$]: During this time interval, $S$ remains on. Diodes $D_1$, $D_3$, $D_4$ and $D_o$ are reverse biased, and $D_2$ and $D_5$ are forward biased. The current-flow path is shown in Fig. 3(b). The magnetizing inductor $L_m$ stores the energy from DC-source $V_{in}$. A part of the energy of DC-source $V_{in}$ is transferred to capacitors $C_2$ and $C_3$ via the coupled inductor. Also, the energies of $C_1$ and $C_4$ are transferred to capacitors $C_2$ and $C_3$ together. Meanwhile, voltages $V_{c2}$ and $V_{c3}$ are approximately equal to $nV_{in}+V_{c3}$. The output capacitor $C_o$ provides its energy to load $R$. This operating mode is ended when switch $S$ is turned off at $t = t_2$.

3) Mode III [$t_2$, $t_3$]: During this time interval, $S$ is turned off to initiate this mode. Diodes $D_1$, $D_3$, $D_4$ and $D_o$ are reverse biased, and $D_2$ and $D_5$ are forward biased. The current-flow path is shown in Fig. 3(c). The energies of leakage inductor $L_k$ and magnetizing inductor $L_m$ are released to the parasitic capacitor $C_{ds}$ of switch $S$. Capacitors $C_2$ and $C_4$ are charged from DC-source $V_{in}$. Output capacitor $C_o$ provides its energy to load $R$. When the capacitor voltage $V_{c1}$ is equal to $V_{in}+V_{c3}$ at $t = t_3$, diode $D_1$ is conducted and this operating mode is ended.

4) Mode IV [$t_3$, $t_4$]: During this time interval, $S$ remains off. Diodes $D_1$, $D_2$, and $D_3$ are forward biased, and $D_4$, $D_5$, and $D_o$ are reverse biased. The current-flow path is shown in Fig. 3(d). The energies of leakage inductor $L_k$ and magnetizing inductor $L_m$ is released to capacitor $C_1$. Thus, the voltage across the switch is clamped at $V_{in}+V_{c1}$. The magnetizing energy of $L_m$ starts to transfer energy to capacitors $C_3$ and $C_4$. The current $i_{L_k}$ decreases quickly. The secondary-side voltage of the coupled inductor $V_{L2}$ continues to charge capacitors $C_2$ and $C_3$ in parallel until the secondary-side current $i_s$ equals zero. Thus, diodes $D_2$ and $D_3$ are cut off at $t = t_4$. This operating mode is ended.

5) Mode V [$t_4$, $t_5$]: During this time interval, $S$ remains off. Diodes $D_1$, $D_3$, $D_4$ and $D_o$ are forward biased, and $D_2$ and $D_5$ are reverse biased. The current-flow path is shown in Fig. 3(e). The energies of leakage inductor $L_k$ and magnetizing inductor $L_m$ is released to capacitor $C_1$. Thus, the voltage across the switch is clamped at $V_{in}+V_{c1}$. A part of the magnetizing-inductor energy is released to capacitors $C_3$ and $C_4$ in parallel. Simultaneously, secondary side voltage $V_{L2}$ is connected with $V_{c2}$ and $V_{c5}$ in series and the energy of DC source $V_{in}$, $L_m$, $C_2$, and $C_5$ is released to output capacitor $C_o$ and load $R$. When primary-side current $i_{L_k}$ is equal to current $i_{Do}$, capacitor $C_1$ starts to discharge.
This mode is ended at $t = t_5$ when $S$ is turned on at the beginning of the next switching period.

Fig. 2 Some typical waveforms of the proposed converter at CCM operation.

Fig. 3 Current-flow path of operating modes during one switching period at CCM operation. (a) Modes I. (b) Modes II. (c) Mode III. (d) Mode IV. (e) Mode V.

(B) DCM Operation

To simplify the analysis of DCM operation, the leakage inductor $L_k$ of the coupled-inductor is neglected. Fig. 4 shows typical waveforms of the proposed converter operated in DCM. There are three modes in DCM operation and Fig. 5 shows the operating stages of each mode. The operating modes are described as follows:
1) Mode I \([t_0, t_1]\): During this time interval, \(S\) is turned on to initiate this mode. The current-flow path is shown in Fig. 5(a). The energy of DC-source \(V_{in}\) is transferred to magnetizing inductor \(L_m\). Thus, \(i_{Lm}\) is increased linearly. Also, the secondary side of the coupled inductor is connected series with capacitor \(C_3\) or \(C_4\) and releases their energies to charge capacitors \(C_2\) and \(C_5\) in parallel. The output capacitor \(C_o\) provides its energy to load \(R\). This mode is ended when \(S\) is turned off at \(t = t_1\).

2) Mode II \([t_1, t_2]\): During this time interval, \(S\) is turned off to initiate this mode. The current-flow path is shown in Fig. 5(b). The energies of DC source \(V_{in}\) and magnetizing inductor \(L_m\) are transferred to capacitors \(C_1\), \(C_o\), and load \(R\). Similarly, capacitors \(C_2\) and \(C_5\) are discharged in series with DC source \(V_{in}\) and magnetizing inductor \(L_m\) to capacitor \(C_o\) and load \(R\). The energy of magnetizing inductor \(L_m\) is transferred to capacitors \(C_3\) and \(C_4\) by coil \(N_c\). This mode is ended when the energy stored in \(L_m\) is empty at \(t = t_2\).

3) Mode III \([t_2, t_3]\): During this time interval, \(S\) remains off. The current-flow path is shown in Fig. 5(c). Since the energy stored in \(L_m\) is empty, the energy stored in \(C_o\) is discharged to load \(R\). This mode is ended when \(S\) is turned on at \(t = t_3\).

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III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

(A) CCM Operation

At modes IV and V, the energy of the leakage inductor \(L_k\) is released to capacitor \(C_1\). According to [19], the energy released duty cycle \(D_{c1}\) can be expressed as

\[
D_{c1} = \frac{t_{c1}}{T_s} = \frac{2(1 - D)}{n + 1},
\]

where \(t_{c1}\) is the time interval of the energy of leakage inductor recycled by capacitor \(C_1\).

By applying the voltage-second balance principle of \(L_k\), the voltage across capacitor \(C_1\) can be expressed as

\[
V_{c1} = D \cdot V_{in} \cdot \frac{(1 + k) + (1 - k) n}{2}.
\]
\[ V_{L_1} = \frac{L_m}{L_m + L_{k1}} V_{in} = kV_{in}, \]  
\[ V_{L_2} = nV_{L_1} = nkV_{in}. \]  

Also, the voltage across capacitors \( C_2 \) and \( C_5 \) can be written as

\[ V_{c2} = V_{L_2} + V_{c3}, \]  
\[ V_{c5} = V_{L_2} + V_{c4}. \]

During the time duration of modes \( V \), the following equations can be formulated based on Fig. 3(e).

\[ V_{L_2} = V_{in} + V_{c1} + V_{c2} + V_{c5} - V_o, \]  
\[ V_{L_2} = -V_{c3} = -V_{c4}. \]

The voltage across magnetizing inductor \( L_m \) can be derived from Equation (6)

\[ V_{L_2} = \frac{V_{L_2}}{n} = \frac{V_{in} + V_{c1} + V_{c2} + V_{c5} - V_o}{n}. \]

By applying the volt-second balance principle on \( N_s \), the following equation is given

\[ \int_0^{T} V_{c2}' dt + \int_0^{T} V_{L_2}' dt = 0. \]

Substituting (4) and (8) into (10), the voltage of capacitors \( C_2 \) and \( C_5 \) are obtained as

\[ V_{c3} = V_{c4} = \frac{Dnk}{1-D} V_o. \]  

And substituting (11) to (5) and (6), the voltage across capacitors \( C_2 \) and \( C_3 \) can expressed as

\[ V_{c2} = V_{c5} = (nk + \frac{Dnk}{1-D}) V_{in}. \]

Also, using the volt-second balance principle on \( N_p \), the following equation is given

\[ \int_0^{T} V_{c2}' dt + \int_0^{T} V_{L_2}' dt = 0. \]

Substituting (2), (3), (9), (11) and (12) into (13), the voltage gain is obtained as

\[ M_{CCM} = \frac{1+2n+nD}{1-D} \]  
\[ \frac{Dnk}{1-D}. \]  

The schematic of the voltage-gain versus the duty-ratio under various coupling-coefficients of the coupled-inductor is shown in Fig. 6. It illustrates that the coupling coefficient results the voltage gain decline. However, voltage gain is less sensitive to the coupling-coefficient. When \( k = 1 \), the ideal voltage gain is written as

\[ M_{CCM} = \frac{1+2n+nD}{1-D} \]

In Fig. 6, the curve shows the voltage gain versus the duty ratio of the proposed converter, and the converters in [26] and [27] at CCM operation under \( k = 1 \) and \( n = 3 \). Since the coupled inductor is worked as flyback and forward converters, voltage gain of the proposed converter is higher than that of the converters in [26] and [27]. Moreover, the utilization rate of the magnetic core of the coupled inductor can be improved.

(B) DCM Operation

In DCM operation, three modes are discussed. The typical waveforms are shown in Fig. 4. In the time duration of mode \( I \), switch \( S \) is turned on. Thus, the following equations can be formulated based on Fig. 5(a)

\[ V_{L_1}' = V_{in}, \]  
\[ V_{L_2}' = nV_{in}. \]
\[ I_{\text{Lmp}} = \frac{V_{\text{in}}}{L_m} DT_s. \] (18)

Furthermore, the voltage across capacitors \( C_2 \) and \( C_3 \) can be written as
\[
V_{c2} = V_{c2}^l + V_{c3}^l, \quad (19)
\]
\[
V_{c3} = V_{c3}^l + V_{c3}^r, \quad (20)
\]

In the time interval of mode II, the following equations can be expressed based on Fig. 5(b):
\[
v_{c1}^l = -V_{c1}^r, \quad (21)
\]
\[
v_{c2}^l = V_{c2}^r + V_{c3}^l - V_{c3}^r. \quad (22)
\]

Also, the voltage across capacitors \( C_3 \) and \( C_4 \) is expressed as
\[
V_{c3} = V_{c4} = -v_{c2}^l. \quad (23)
\]

During the time interval of mode III, the following equation can be derived from Fig. 5(c):
\[
v_{c1}^{III} = v_{c2}^{III} = 0. \quad (24)
\]

By applying the voltage-second balance principle on coupled inductor, the following equations are given as
\[
\int_{0}^{DT_s} v_{c1}^l dt + \int_{0}^{DT_s} v_{c1}^r dt + \int_{0}^{DT_s} v_{c1}^{III} dt = 0, \quad (25)
\]
\[
\int_{0}^{DT_s} v_{c2}^l dt + \int_{0}^{DT_s} v_{c2}^r dt + \int_{0}^{DT_s} v_{c2}^{III} dt = 0. \quad (26)
\]

Substituting (17), (23) and (24) into (25), the voltage is obtained as
\[
V_{c3} = V_{c4} = -\frac{nD}{D_L} V_{\text{in}}, \quad (27)
\]

Similarly, substituting (16), (19), (20), (21), (22), (24) and (27) into (25), the voltage across capacitors \( C_1, C_2 \) and \( C_3 \) is derived as
\[
V_{c1} = \frac{D}{D_L} V_{\text{in}}, \quad (28)
\]
\[
V_{c2} = V_{c3} = (n+1) \frac{nD}{D_L} V_{\text{in}}, \quad (29)
\]

Also, the voltage gain is expressed as
\[
V_o = \frac{D}{D_L} (3n+1) + (2n+1) V_{\text{in}}. \quad (30)
\]

According to (30), the duty cycle \( D_L \) can be derived as
\[
D_L = \frac{(1+3n)DV_{\text{in}}}{V_o - (1+2n)V_{\text{in}}}. \quad (31)
\]

From Fig. 4, the average value of \( i_{c0} \) is computed as
\[
I_{c0} = \frac{1}{2} D_L \frac{I_{\text{Lmp}}}{3n+1} - I_a. \quad (32)
\]

Since \( I_{c0} \) is equal to zero under steady state, equations (18), (31), and \( I_{c0} = 0 \) can be substituted to (32). Thus, equations (32) can be rewritten as follows:
\[
\frac{D^2 L_m V_o^2 T_s}{2[V_o - (1+2n)V_{\text{in}}] L_m} = \frac{V_o}{R}. \quad (33)
\]

Then, the normalized magnetizing-inductor time constant is defined as
\[
\tau_{Lm} = \frac{L_m}{RT_s} = \frac{L_m f_s}{R}, \quad (34)
\]

where \( f_s \) is the switching frequency. Substituting (34) into (33), the voltage gain is given by
\[
M_{\text{DCM}} = \frac{V_o}{V_{\text{in}}} = \frac{1+2n}{2} + \frac{(1+2n)^2}{4} \frac{D^2}{2\tau_{Lm}}. \quad (35)
\]

The curve of the voltage gain is shown in Fig. 8 which illustrates the voltage-gain versus the duty-ratio under various \( \tau_{Lm} \).

![Fig. 8 Voltage-gain versus duty-ratio at DCM operation under various \( \tau_{Lm} \) and at CCM operation under \( n = 3 \) and \( k = 1 \).](image)

(C) Boundary Operating Condition between CCM and DCM

If the proposed converter is operated in boundary condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. The boundary normalized magnetizing-inductor time constant \( \tau_{LmB} \) can be derived from (15) and (35) as
\[
\tau_{LmB} = \frac{D(1-D)^2}{2(1+3n)(1+2n+nD)}. \quad (36)
\]

The curve of \( \tau_{LmB} \) is plotted in Fig. 9. If \( \tau_{Lm} \) is larger than \( \tau_{LmB} \), the proposed converter is operated in CCM.
Substituting equation (45) into (46) and (47), the following equation is derived as switch is on:

\[ I_{c2\text{\(\text{on}\)}}} = I_{c5\text{\(\text{on}\)}} = \frac{1-D}{D} I_o \tag{48} \]

Also, the energy of \(C_2\) and \(C_5\) are provided by capacitor \(C_3\) and \(C_4\). The following equation can be derived as

\[ I_{c3\text{\(\text{on}\)}}} = I_{c2\text{\(\text{on}\)}} = \frac{1-D}{D} I_o \tag{49} \]
\[ I_{c4\text{\(\text{on}\)}}} = I_{c5\text{\(\text{on}\)}} = \frac{1-D}{D} I_o \tag{50} \]

Using the current-balance principle on capacitors \(C_3\) and \(C_4\), the current is derived as

\[ I_{c3\text{\(\text{off}\)}}} = I_{c4\text{\(\text{off}\)}} = I_o \tag{51} \]

The average current of diodes \(D_2-D_5\) can be derived from charged-current of capacitor \(C_2-C_5\). Thus, the following equation are given as

\[ i_{D2\text{\(\text{peak}\)}}} = i_{D5\text{\(\text{peak}\)}} = \frac{2V_o}{DR} \tag{52} \]
\[ i_{D3\text{\(\text{peak}\)}}} = i_{D4\text{\(\text{peak}\)}} = i_{D6\text{\(\text{peak}\)}} = \frac{2V_o}{(1-D)R} \tag{53} \]

The current flow through the switch based on fig. 3(b) is expressed as

\[ i_{d(s)} = n(i_{D2\text{\(\text{peak}\)}}} + i_{D5\text{\(\text{peak}\)}}} + I_{\text{\(\text{cap}\)}} \tag{54} \]

Also, when switch is turned off, the peak current of switch is equal to the current of diode \(D_1\).

Substituting (32), (56) into (58), the peak current value of switch and diode \(D_1\) are expressed as

\[ i_{d(s)} = i_{D1\text{\(\text{peak}\)}}} = \frac{2(D + Dn + 2n)V_o}{(1-D)DR} \tag{55} \]

If the converter is operating at CCM, the current stress is modified to
\[
\begin{align*}
    i_D2(\text{peak}) &= \frac{2I_{a(BCM)}}{D} + \frac{I_o - I_{a(BCM)}}{1-D} \\
    i_D3(\text{peak}) &= i_Do(\text{peak}) = \frac{2I_{a(BCM)}}{(1-D)} + \frac{I_o - I_{a(BCM)}}{D} \\
    i_Dh(\text{peak}) &= i_{Dh(\text{peak})} = \frac{2(D + Dn + 2n)I_{a(BCM)}}{(1-D)D} + \frac{(2Dn + 1 - D)(I_o - I_{a(BCM)})}{D(1-D)}
\end{align*}
\]

IV. EXPERIMENTAL RESULTS OF THE PROPOSED CONVERTER

To verify the performance of the proposed converter, a prototype circuit is implemented in the laboratory. The specifications are as follows:

1) input DC voltage \( V_{in} \): 24 V
2) output DC voltage \( V_o \): 400 V
3) maximum output power: 200 W
4) switching frequency: 50 kHz
5) MOSFET \( S \): IRFB4410ZPBF
6) Diodes \( D_1 \): MBR30100CT, \( D_2/D_3/D_4/D_5/D_o \): DESP30
7) Coupled inductor: ETD-59, core pc40, \( N_p : N_s = 1 : 2 \)
8) Capacitors \( C_1/C_2/C_3/C_4/C_5 : 22 \ \mu F/200 \ \text{V}, C_o : 150 \ \mu F/450 \ \text{V}\)

Fig. 10 shows the measured waveforms for full-load \( P_o = 200 \ \text{W} \) and \( V_{in} = 24 \ \text{V} \). The proposed converter is operated in CCM under full-load condition. In the measured waveforms, the \( V_{ds} \) is clamped at appropriately 93 V during the switch-off period. The waveforms demonstrate that the steady-state analysis is correct. Therefore, the low-voltage rated switch can be adopted to achieve high efficiency for the proposed converter.

The waveform of secondary-side current \( i_s \) in Fig. 10(a) shows that the proposed converter is operated in CCM because the current is not equal to zero when the switch is turned on. In Fig. 10(b), the waveforms of \( i_{D2} \) and \( i_{D3} \) show that capacitors \( C_2 \) and \( C_3 \) are charged in the different time durations. Capacitors \( C_2 \) and \( C_4 \) are charged in parallel when switch is turned on. Capacitors \( C_3 \) and \( C_5 \) are charged in parallel during the switch-off period and capacitors \( C_2 \) and \( C_5 \) are discharged in series in the same time. Fig. 10(c) shows that the energy of leakage inductor \( L_k \) is released to capacitor \( C_1 \) through diode \( D_1 \). Fig. 10(d) reveals that \( V_{c1}, V_{c2} \) and \( V_{c3} \) satisfy Equations (2), (11) and (12). In addition, output voltage \( V_o \) is consistent with Equation (15). Fig. 10(e) shows the voltage stress of main switch and diodes, and demonstrates the consistency of Equations (38), (39), (41), (42) and (43). The reverse-recovery problem is also alleviated by coupled-inductor. Fig. 11 shows the experimental conversion efficiency of the proposed converter. Maximum efficiency is around 95.28% at \( P_o = 80 \ \text{W} \) and \( V_{in} = 24 \ \text{V} \). The full-load efficiency is appropriately 93.8 % at \( P_o = 200 \ \text{W}, V_{in} = 24 \ \text{V} \), and \( V_{out} = 400 \ \text{V} \).
analyses of voltage gain and boundary operating condition are discussed. Finally, a prototype circuit of the proposed converter is implemented in the laboratory. Experimental results verify the analysis. The conversion efficiency is 95.28%. Also, the reverse-recovery problem of diodes is alleviated by coupled-inductor. The voltage stress on the main switches is 93 V. Low voltage ratings and low on-state resistance levels $R_{D(ON)}$ Switch can be selected. The proposed converter is suitable for low-voltage source to grid connection.

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Yi-Ping Hsieh was born in Tainan, Taiwan, in 1986. He received the B.S. degree and the M.S. degree in electrical engineering from national Cheng-Kung University (NCKU), Taiwan, in 2008 and 2010, respectively. He is currently pursuing a Ph.D. degree at NCKU, Taiwan. His research interests are power factor correction, DC/DC power converter, DC/AC inverter, renewable energy conversion, LED lighting and electronic ballast.

Jiann-Fuh Chen (S‘79–M’80) was born in Chung-Hua, Taiwan, in 1955. He received his B.S., M.S. and Ph.D. degrees in electrical engineering from NCKU in 1978, 1980 and 1985, respectively. Since 1980, he has been with the department of Electrical Engineering at NCKU, where he is currently a professor. His research interests are power electronics and energy conversion.

Tsong-Juu (Peter) Liang (M’93–SM’10) was born in Kaohsiung, Taiwan. He received his B.S. degree in Electrophysics from National Chiao-Tung University, Hsinchu, Taiwan, in 1985. He received his M.S. and Ph.D. degrees in Electrical Engineering from the University of Missouri, Columbia, USA, in 1990 and 1993, respectively. He is currently a Professor of Electrical Engineering and Director of Green Energy Electronics Research Center (GEERC), National Cheng-Kung University (NCKU), Tainan, Taiwan. Currently, he is the Associate Editor of IEEE Trans. on Power Electronics, the Associate Editor of IEEE Trans. on Circuits and Systems-I, and the Technical Committee Chair of IEEE CAS Systems Power and Energy Circuits and Systems Technical Committee. He is also on the Board of Directors for Compucase Enterprise Co., Ltd and Catcher Technology Co., Ltd.

Lung-Sheng Yang was born in Tainan, Taiwan, R.O.C., in 1967. He received the B.S. degree in electrical engineering from National Taiwan Institute of Technology, Taiwan, the M.S. degree in electrical engineering from National Tsing-Hua University, Taiwan, and the Ph.D degree in electrical engineering from National Cheng-Kung University in 1990, 1992, and 2007 respectively. He is currently with the Department of Electrical Engineering, Far East University, Tainan, where he is an assistant professor. His research interests are power factor correction, dc–dc converters, renewable energy conversion, and electronic ballasts.