Comparison of low-temperature GaN, SiO$_2$, and SiN$_x$ as gate insulators on AlGaN/GaN heterostructure field-effect transistors

C. J. Kao, M. C. Chen, C. J. Tun, and G. C. Chi
Department of Physics and Institute of Optical Science, National Central University, Chung-Li 32054, Taiwan

J. K. Sheu
Institute of Electro-optical Science and Engineering, National Cheng Kung University, Tainan 70101, Taiwan

W. C. Lai and M. L. Lee
Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan

F. Ren
Department of Chemical Engineering, University of Florida, Gainesville, Florida 32611

S. J. Pearton$^{a}$
Department of Materials Science and Engineering, University of Florida, Gainesville, Florida 32611

(Received 10 March 2005; accepted 9 August 2005; published online 27 September 2005)

The performance of AlGaN/GaN heterostructure field-effect transistors (HFETs) with either uncapped surfaces or with low-temperature (LT) GaN or SiO$_2$ or SiN$_x$ as gate insulators is reported. The sheet carrier concentrations of AlGaN/GaN HFETs with any of these surface insulating layers are similar to each other and in each case about 50% higher than that in an AlGaN/GaN HFET with a free surface. This result is consistent with the insulator layers providing passivation of surface states that cause the depletion of the channel layer. Due to the closer lattice match with the AlGaN surface layer, the HFET with a LT-GaN layer as the gate insulator shows the best dc and rf device performance, demonstrating that this material is an effective insulator for nitride electronic devices. © 2005 American Institute of Physics. [DOI: 10.1063/1.2058173]

INTRODUCTION

The recent progress in the development of AlGaN/GaN heterojunction field-effect transistors (HFETs) for high-frequency and high-power applications has been very rapid.$^{1-6}$ The wide band gap and high breakdown voltage of this materials system means that AlGaN/GaN HFETs have enormous potential for uncooled operation in high-temperature environments. These devices are capable of producing very high microwave power densities (>12 W/mm), along with high breakdown voltage and low noise figures. In order to improve the performance for high-power, high-temperature applications, insulating gate layers are widely employed to reduce gate leakage current, increase operating voltage, and protect the device surface.$^5-10$ The use of gate insulators for compound semiconductor electronics would alleviate many of the problems encountered in current Schottky-based devices, such as poor thermal stability. Furthermore, circuit design can be simplified since enhancement-mode metal-oxide-semiconductor field-effect transistors (MOSFETs) can be used to form single-supply voltage control circuits for power transistors. The use of MOSFETs also allows the use of complementary devices, thus producing less power consumption and allowing for simpler circuit design. Many reports have indicated that using a gate insulator on AlGaN/GaN HFETs might cause enhancement of the carrier density in the channel. This can be explained if the surface insulating layers reduce surface-state-related depletion of the channel layer.$^{10}$ In previous works, SiO$_2$, SiN$_x$, AlN, Ga$_2$O$_3$, Sc$_2$O$_3$, Gd$_2$O$_3$, Ta$_2$O$_5$, and some polymer substances have all been used as the insulating material of nitride-based HFETs.$^5-26$ Another possibility as the gate insulator is GaN grown at low temperature (LT-GaN). This is a common nucleation layer for GaN growth on sapphire but has poor crystalline quality and very high resistivity.$^{27-31}$ It has quite different electrical properties from high-temperature-grown GaN layers and has been used as a stable insulating gate layer for nitride-based devices.$^{32-36}$ Using LT-GaN as the insulating layer of nitride-based devices has the advantage of growth within the same metal-organic chemical-vapor deposition (MOCVD) system as the active layers of the HFET structure, which avoids surface contamination. In addition, the close lattice match with the nitride-based device layers reduces strain effects. In this study, LT-GaN, SiO$_2$, and SiN$_x$ are compared as insulating gate layers on AlGaN/GaN HFETs.

EXPERIMENT

Samples used in this study were all grown on c-face (0001) sapphire substrates in a vertical geometry MOCVD reactor.$^{37,38}$ Silane (SiH$_4$) and bicyclopentadienyl magnesium (Cp$_2$Mg) were used as the n-type and p-type doping sources, respectively. A 30-nm-thick GaN nucleation layer

$^a$Electronic mail: spear@mse.ufl.edu
was first grown on top of the sapphire substrate at 560 °C. The temperature was then raised to 1060 °C to grow a 2-μm-thick undoped GaN (n ~ 3 × 10^{16} cm^{-3}) buffer layer. On top of the buffer layer, a 50-nm-thick Mg-doped GaN layer was grown to eliminate substrate leakage current and enhance the pinch-off characteristics. A 0.3-μm-thick undoped GaN was then grown at 1060 °C to serve as the channel layer. A 5-nm-thick undoped Al_{0.25}Ga_{0.75}N spacer and a 30-nm-thick Si-doped Al_{0.25}Ga_{0.75}N barrier layers (n ~ 1 × 10^{18} cm^{-3}) were subsequently grown as the doped regions in the structure. Finally, a 20-nm-thick LT-GaN high-resistivity capping layer was grown on top of the barrier layer at 560 °C. The sample with this structure is labeled sample B. The sample without the LT-GaN capping layer prepared under the same conditions to compare with Sample B is labeled sample A. For the gate insulator comparison, a 20-nm-thick SiO_{2} or SiN_{x} cap layer was grown on sample A by plasma-enhanced chemical-vapor deposition (PECVD). A piece of sample A with either a 20-nm-thick SiO_{2} or SiN_{x} capping layer was labeled sample C or sample D, respectively. The schematics of samples A, B, C, and D are provided in Fig. 1.

Hall-effect measurements were used to obtain the carrier concentration, using 5 × 5 mm^{2} dimension samples with Van der Pauw patterns. The contact areas were defined by photolithography. For samples B, C, and D, extra etching processes to remove the high-resistivity capping layers above the Ohmic contact areas were achieved by inductively coupled plasma (ICP) etching. Ti/Al/Ti/Au (50/100/50/200 nm) multilayer metal was deposited by e-beam evaporation and patterned as Ohmic contacts on the exposed Si-doped Al_{0.25}Ga_{0.75}N barrier layer of each sample.

In order to study the electrical characteristics, metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HFETs) were fabricated. Mg ions were implanted into the samples for electrical isolation and also for defining active areas. After the source/drain Ohmic contact regions were defined on the active areas by photolithography, addi-
tional plasma etching processes were used on samples B, C, and D to etch away the capping insulators in the Ohmic contact areas. The Ti/Al/Ti/Au (50/100/50/200 nm) multilayer metal was deposited onto the exposed Al$_{0.25}$Ga$_{0.75}$N barrier layer to serve as source/drain electrodes. Finally, Ni/Au (100/100 nm) Schottky contacts were deposited on the gate areas to serve as the gate electrodes. For sample A, the gate electrode was deposited on top of the Al$_{0.25}$Ga$_{0.75}$N barrier layer. For samples B, C, and D, the gate electrodes were located on top of the different insulating gate layers. A scanning electron micrograph of a completed device from sample B is shown in Fig. 2. The gate length and width on the fabricated device are 0.5 and 100 $\mu$m, respectively. The device dc electrical characteristics were measured at room temperature by using an Agilent 4156C semiconductor parameter analyzer.

**RESULTS AND DISCUSSION**

Figure 3 compares the sheet carrier concentrations ($n_s$) as a function of temperature in the four samples. In samples B, C, and D, the sheet carrier concentrations are similar and about 50% higher than the free-surface structure, sample A. This result is consistent with these insulator layers changing the electronic density of states at the Al$_{0.25}$Ga$_{0.75}$N barrier layer surface and reducing the surface-related depletion of the channel layer. This phenomenon can be thought of as the insulator layers providing partial passivation of surface states on the Al$_x$Ga$_{1-x}$N surface. The LT-GaN cap layer of sample B has a very high resistivity, larger than $10^{11}$ $\Omega$/$\square$. From past works, it is known that the LT-GaN is a highly compensated material, due to the deep acceptor states originating from the high density of structural impurities. A theoretical model for the electron density of states can be used to understand the band structure of AlGaN/GaN heterostructures. It was found that the AlGaN barrier layer provides a large band gap and thereby minimizes the electron leakage through the barrier, resulting in lower leakage currents and higher breakdown voltages.

Figure 4 shows the $I_{DS}$-$V_{DS}$ characteristics with changing gate bias of the four devices: (a) uncapped, (b) LT-GaN insulator, (c) SiO$_2$ insulator, and (d) Si$_3$N$_4$ insulator.
defects. Therefore, this result differs from that in the conventional GaN/Al$_{x}$Ga$_{1-x}$N/GaN heterostructure. In that case, high-temperature-grown GaN cap layers produce a reduction in sheet carrier concentration.

dc electrical characteristics of the MIS-HFETs are shown in Figs. 4(a)–4(d). The drain-source current/drain-source voltage ($I_{DS}$-$V_{DS}$) characteristics were measured at room temperature in the dark. The pinch-off characteristics in all of the devices are excellent due to the presence of the 50-nm-thick Mg-doped layer. The typical threshold voltages were around −2.5, −8, −17, and −19 V in samples A, B, C, and D, respectively. Compared with sample A, the larger threshold voltages in samples B, C, and D were attributed to the larger distance between the gate metal and undoped GaN channel layer caused by the insertion of the insulating gate layers.

Figure 5 shows the comparison of drain-source saturation currents ($I_{DSS}$) when the gate bias ($V_{GS}$) is at 0 V. Samples B, C, and D have $I_{DSS}$ of 495, 217, and 215 mA/mm, respectively. Those currents are higher than the $I_{DSS}$ of 94 mA/mm in sample A. This result may be attributed to the increase in effective carrier concentration in the channel in samples with insulating gate layers. From a comparison of the current ramps and the saturation currents of those samples, the different influences of the insulating cap layers become evident. Compared with sample A, the structures with an insulating cap layer have a lower surface-state density that reduces the surface-related depletion effects. Moreover, the structure with a LT-GaN capping layer (sample B) has a superior dc performance to the other two insulator capping layer structures. This may be attributed to the better lattice match with the underlying Al$_{0.25}$Ga$_{0.75}$N surface layer and the absence of contamination that might occur on moving the samples from the MOCVD reactor to the PECVD system.

In Fig. 6, the transfer characteristics from all four samples are shown. The transconductance ($g_m$) values are plotted as a function of $V_{GS}$. The $g_m$ profiles of samples B, C, and D are broader than that of sample A. This is consistent with the fact that the Schottky gate metal on the samples with insulating cap layers was further away from the current channel layer. The broad $g_m$ profile could in turn result in a larger gate voltage swing, improving the linearity and the dynamic range of output power. The maximum $g_m$ of samples A, B, C, and D are 40, 72, 16 and 18 mS/mm, respectively. The current driving ability of sample B is superior to the others. Although all of the samples with insulating cap layers produced higher drain-source saturation currents, samples C and D still could not achieve a high $g_m$ performance, which may be caused by contamination at the SiO$_2$–SiN$_x$–Al$_{0.25}$Ga$_{0.75}$N interfaces and the strain induced by these dielectrics on samples C and D, respectively.

$S$-parameter measurements were performed for samples A and B. In Fig. 7, the corresponding current gain ($h_{21}$), maximum stable gain (MSG), and maximum available gain (MAG) are given from the $S$-parameter measurement as a function of frequency. The $f_T/f_{max}$ values in samples A and B are 9.7/14.4 and 19.4/33.8 GHz, respectively. The $f_T$ and $f_{max}$ enhancements in sample B also could be attributed to the higher transconductance, which is caused by the influence of the LT-GaN capping layer.

SUMMARY AND CONCLUSIONS

In this study, the influence of LT-GaN/SiO$_2$/SiN$_x$ as gate insulators on AlGaN/GaN HFETs was studied. The
high-resistivity capping layers reduce the electronic density of states at the interface with Al0.25Ga0.75N. This leads to a reduction of surface-related depletion of the channel layer and increases the sheet carrier concentration by about 50%. AlGaN/GaN MIS-HFETs with and without gate insulators were also fabricated. Although the samples with insulating layers all exhibited higher drain-source saturation currents, samples C and D showed poorer current driving ability. This suggests that PECVD SiO2 and SiN4 are not suitable gate insulators for AlGaN/GaN HFETs. By contrast, LT-GaN has the advantage of reduced surface contamination and improved lattice match with the AlGaN/GaN HFET active layers. The Al0.25Ga0.75N HFET with a LT-GaN gate insulator exhibited excellent dc and rf characteristics. These results suggest that LT-GaN may be a good choice as the gate insulator on AlGaN/GaN FETs.

ACKNOWLEDGMENTS

The authors would like to thank the National Science Council of Taiwan (R.O.C.) for financially supporting this research. The work at UF is partially supported by NSF (CTS-0301178, monitored by Dr. M. Burka and Dr. D. Senich), by NASA Kennedy Space Center Grant No. NAG 10-316 monitored by Mr. Daniel E. Fitch, and by NSF DMR 0400416.