Bimetallic oxide nanoparticles Co$_x$Mo$_y$O as charge trapping layer for nonvolatile memory device applications

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The reduced Co$_x$Mo$_y$O bimetallic oxide nanoparticles (BONs) embedded in the hafnium oxynitride high-k dielectric have been developed by means of the chemical vapor deposition method. Capacitance-voltage (C-V) measurements estimate that a charge trap states density of 1.1 $\times 10^{12}$ cm$^{-2}$ and a flatband voltage shift of 700 mV were achieved during the C-V hysteresis sweep at $\pm$5 V. Scanning electron microscopy image displays that the Co$_x$Mo$_y$O BONs with a diameter of $\sim$4–20 nm and a surface density of $\sim1 \times 10^{11}$ cm$^{-2}$ were obtained. The writing characteristics measurements illustrate that the memory effect is mainly due to the holes trapping. © 2007 American Institute of Physics. [DOI: 10.1063/1.2763962]

High-performance nonvolatile memory (NVM) devices with a polycrystalline silicon-oxide-nitride-oxide-silicon (SONOS) structure have been demonstrated. However, the conventional thin films as charge trapping layers (CTLs) of the SONOS devices need to overcome the problems of the charge loss due to a local leakage path. In addition, the metal gate and high-dielectric-constant (high-k) gate oxides with equivalent-oxide thickness (EOT) have been widely used to supersede the tunneling oxide of the silicon dioxide (SiO$_2$) for reducing gate leakage current. Therefore, the nanoparticles (NPs) embedded in the high-k gate dielectric would be an attractive technology option for the NVM device applications. Recently, several approaches related to NPs as CTLs have been achieved such as Si, Ge, Au, Pt, NiSi$_2$, W, TiN, Ni, and Al$_2$O$_3$ NPs. The flatband voltage shift of 600 mV is obtained in self-organized Ge NPs embedded with equivalent-oxide thickness (EOT) of 6 nm and a flatband voltage shift of $\pm$700 mV were achieved during the C-V hysteresis sweep at $\pm$5 V. Scanning electron microscopy image displays that the Co$_x$Mo$_y$O BONs with a diameter of $\sim$4–20 nm and a surface density of $\sim1 \times 10^{11}$ cm$^{-2}$ were obtained. The writing characteristics measurements illustrate that the memory effect is mainly due to the holes trapping.

An Al/HfON/Co$_x$Mo$_y$O NPs/HfON stack structure was formed on a (100)-oriented $p$-type silicon substrates for the metal-oxide semiconductor (MOS) capacitors fabrication. Prior to HfON growth, all wafers were cleaned with a wet cleaning process [APM($=$NH$_4$OH/H$_2$O$_2$/H$_2$O)/HPM ($=$HCl/H$_2$O$_2$/H$_2$O)/DHF($=$HF/H$_2$O)]. Then, the Hf layers were deposited via sputtering and patterned by the lift-off method.

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technique. Finally, the backsides of all samples were also deposited with a 500 nm thick Al film by thermal evaporation following the oxide stripping. The morphology and the compositions of the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ NPs were analyzed by means of the scanning electron microscopy (SEM) and the energy dispersive spectrometry (EDS) of the transmission electron microscopy (TEM), respectively.

Typical capacitance-voltage (C-V) hysteresis sweep of the MOS devices with and without the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs were investigated, as shown in Fig. 1. No clear hysteresis shift between the forward (from inersion to accumulation) and the reverse (from accumulation to inversion) C-V curve can be observed for the NP-0 min sample even under at ±10 V sweep. On the contrary, the flatband voltage shift ($\Delta V_{fb}$) of 0.3, 0.7, and 1.5 V were obtained for the NP-15 min sample under ±3, ±5, and ±10 V hysteresis sweeps, respectively, as shown in the inset of Fig. 1. Therefore, Fig. 1 suggests that the flatband voltage shift ($\Delta V_{fb}$) can be achieved by the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs embedded in the HfON high-$k$ dielectrics. In addition, compared to the NP-0 min sample, the C-V curves of the NP-15 min sample shift to the left, indicating that the positive charges (holes trapping) are generated in the gate dielectric bulk, due to the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs as CTLs of the NVM devices. Furthermore, to estimate the charge trap states densities of the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs, the following equation was adopted: $N = (C_{eff}/qA)\Delta V_{fb}$, where $C_{eff}$ is the capacitance of the MOS devices with the HfON/Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$/MOX stack dielectric, $q$ is the electronic charge and equal to 1.6 $\times$ 10$^{-19}$ C, $A$ is the area of the MOS devices, and $\Delta V_{fb}$ is the flatband voltage shift due to hysteresis sweep. For the MOS devices with $C_{eff} = 320$ pF, $A = 0.001256$ cm$^2$, and $\Delta V_{fb} = 0.7$ V, the charge trap states density is estimated to be around 1.1 $\times$ 10$^{12}$ cm$^{-2}$ during the C-V hysteresis sweep at ±5 V.

Figure 2 shows that (a) the morphology and (b) the composition of the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs were detected by the (a) SEM and (b) EDS of the TEM, respectively. The cross section of the SiO$_2$/Pd/Pt/Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$/HfON structure was shown in the inset of figure (b). In order to prevent the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs peeling off the HfON surface, the SiO$_2$/Pd/Pt capping layer was used. Then, the cross section sample was prepared by the focus ion beam. The peaks of the Si, Pd, and Pt were detected due to the SiO$_2$/Pd/Pt capping layer.

FIG. 1. Typical capacitance-voltage (C-V) hysteresis characteristics of the memory devices with and without the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs were obtained. The C-V sweep loops included ±3, ±5, and ±10 V. The inset figure examines the flatband voltage shift as function of the various sweep loops.

In this work, the larger diameter NPs could be consist of the CoO and Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ agglomeration in an Ar/NH$_3$ ambient. Additionally, the EDS result from a TEM instrument shows that the composition of the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs in this work is around Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$.

Figure 3(a) displays the band diagrams of the electrons and holes injection operation using +5 and −5 V, respectively. During a +5 V biased at the control gate, the electrons directly tunnel from the Si substrate through the HfON tunnel oxide, and are trapped in the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs. On the contrary, as a −5 V biased at the control gate, the holes were injected into the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs or the electrons erase back to the Si substrate. Further programing properties of the MOS devices with the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs under various programing times were shown in Fig. 3(b). After a ±5 V biased voltage with various programing times, all C-V curves were measured from +3 to −3 V. The results suggest that the flatband voltage has little shift to left with the increase of the programing times for the electrons injection condition, indicating that the electrons are difficult to be written into the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs. On the contrary, with increasing the programing times, a clear shift to the left can be observed for a negative programing voltage of −5 V, suggesting that the holes are much easier to be written into the Co$_{0.40}$Mo$_{0.45}$O$_{0.15}$ BONs.
shown in Fig. 4. The results show that the memory window could be due to the higher work function of Co and Mo. Moreover, compared to the NVM device programed at ±5 V hysteresis sweep, the average collection of each Co$_x$Mo$_y$O BONs can be estimated around ten electrons or equivalent holes charges. The writing characteristics measurements illustrated that the memory effect is mainly due to the holes trapping.

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