Properties of Pt/SrBi$_2$Ta$_2$O$_9$/BL/Si MFIS Structures Containing HfO$_2$, SiO$_2$, and Si$_3$N$_4$ Buffer Layers

Ching-Chich Leu,$^{a,b,c}$ Chia-Feng Leu,$^c$ Chao-Hsin Chien,$^d$ Ming-Jui Yang,$^e$ Rui-Hao Huang,$^e$ Chen-Han Lin,$^a$ and Fan-Yi Hsu$^c$

$^a$Department of Chemical and Materials Engineering, National University of Kaohsiung, Kaohsiung 811, Taiwan
$^b$Center for Micro/Nano Science and Technology, National Cheng Kung University, Taiwan
$^c$Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 30043, Taiwan
$^d$Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan
$^e$National Nano Device Laboratories, Hsinchu 30043, Taiwan

The physical and electrical properties of Pt/SrBi$_2$Ta$_2$O$_9$ (SBT)/buffer layer (BL)/Si metal/ferroelectric/insulator/semiconductor (MFIS) structures incorporating HfO$_2$, SiO$_2$, and Si$_3$N$_4$ as buffer layers were investigated. When employing HfO$_2$ as the buffer layer, an MFIS structure exhibiting a high memory ratio was constructed, presumably because of the SBT characteristics and the high quality of the HfO$_2$ layer on the Si substrate. This study demonstrates that HfO$_2$ is one of the best buffer-layer materials for ferroelectric memory applications.

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In recent years, metal/ferroelectric/semiconductor field-effect transistor (MFSET)-type ferroelectric random access memories (FeRAMs) have received much attention because of their many important features, such as their nonvolatility, nondestructive read-out (NDR), low power consumption, and obeying of scaling-down rules.$^{1,2}$ Nevertheless, such MFSET gate structures exhibit some serious problems that affect their memory applications, such as poor interface properties, high leakage currents, inadequate retention, and rapid fatigue. Consequently, metal/ferroelectric/insulator/semiconductor (MFIS) structures, i.e., those incorporating an insulating buffer layer (BL) comprised of SiO$_2$, Si$_3$N$_4$, ZrO$_2$, or CeO$_2$ have been proposed to significantly improve upon these issues.$^{3,4}$ Even with the various buffer layers, the MFIS structures still exhibit large absorption currents because of the existence of a high density of defects or carrier traps on the interface between the Si and buffer layer. In addition, the insertion of an insulating layer results in a further voltage drop across this layer; this phenomenon, therefore, reduces the effective electric field on the ferroelectric film. As a result, a large operation voltage must be applied to the whole device to achieve the saturated polarization of ferroelectrics.

In this present study, we employed three kinds of insulating layers to fabricate MFIS capacitors having Pt/SrBi$_2$Ta$_2$O$_9$/BL/Si (p-type) structures. We deposited a thin (ca. 3.2 nm) HfO$_2$ layer, through atomic vapor deposition (AVD), that satisfied the following requirements: (i) a sufficiently high $k$ value and thickness so that it would not consume a significant portion of the gate voltage, (ii) good thermal stability, and (iii) good BL–Si interfacial properties.$^{5,6}$ By using HfO$_2$ as the buffer layer, the memory window of the stack structure could reach as high as 4.9 V at a sweeping voltage of ±4 V. This memory window is much larger than those obtained when using either SiO$_2$ or Si$_3$N$_4$ as the buffer layer; reasons for these behaviors are suggested below.

The HfO$_2$ layer was deposited at a measured thickness of ca. 3.2 nm through AVD using an AIXTRON Tricent system at a substrate temperature of 500°C under an O$_2$ ambient.$^{13}$ A precleaned, hydrofluoric acid (HF)-dipped p-type silicon (100) wafer was employed as the starting substrate. For HfO$_2$ densification, postdeposition annealing was performed under N$_2$ at 1000°C for 30 s. For comparison, SiO$_2$ and Si$_3$N$_4$ layers having thicknesses of ca. 2.0 and 2.2 nm, respectively, were also employed as buffer layers. These two buffer layers were prepared using thermal oxidation and low-pressure chemical vapor deposition (LPCVD) methods, respectively. SrBi$_2$Ta$_2$O$_9$ (SBT) films (ca. 200 nm thick) were then deposited on top of each buffer layer using a spin-on method and a presynthesized metal organic deposition (MOD) solution; the samples subsequently underwent rapid thermal annealing (RTA) at 750°C under O$_2$ for 1 min. These processes were followed by the deposition of Pt to form both the gate electrode and the back contact.

Figure 1 displays X-ray diffraction (XRD) patterns of the SBT/BL/Si structures annealed at 750°C for 1 min. For convenience, we denote the samples containing the HfO$_2$, SiO$_2$, and Si$_3$N$_4$ buffer layers as samples A, B, and C, respectively. Figure 1 indicates that, regardless of the nature of the buffer layer, the SBT films exhibited polycrystalline bismuth-layered-structure (BLS) phases without any detectable secondary phase.$^{14}$ In addition, the X-ray spectra were virtually identical, with the exception being that the intensity of sample C was slightly lower than those of the other two samples. The scanning electron microscopy (SEM) surface images of these three specimens (Fig. 2a) indicate that the SBT films comprised mainly ellipse-shaped grains having grain sizes of ca. 50–100 nm. These SBT microstructures had smaller and more uniform grains than those we prepared previously on top of a Pt bottom...
electrode. Cross-sectional transmission electron microscopy (Fig. 2b) images indicate that the grains were distributed uniformly throughout SBT films.

Figure 3a displays the high-frequency (100 kHz) capacitance–voltage (C–V) curves of the MFIS structures containing the various buffer layers. The clockwise hysteresis loops (as traced by the arrows) clearly indicate that the memory effects originated from the ferroelectric domain reversion. Large memory windows (5.5 V) existed in specimen A at a sweeping voltage of ±6 V. Figure 3b presents the width of the memory windows as a function of the applied voltage. The memory window of sample A exhibited a near-linear relationship with respect to the applied voltage in the low-voltage region; it increased abruptly, however, from 2.9 to 4.9 V, upon increasing the applied voltage from 3 to 4 V, before reaching saturation. The estimated ratio of the memory window (4.9 V) to the applied voltage (±4 V) is ca. 62%. This surprisingly high value suggests that the electric field on the SBT was sufficiently large to efficiently switch the polarization of domains at such a low operation voltage. In contrast, the memory windows of specimens B (0.12 V) and C (0.21 V) were much lower. Furthermore, in these two samples, we observed no significant changes in the values of memory window (Fig. 3b) upon increasing the applied voltage. This result suggests that the polarizations of the SBT films in samples B and C both remained nonswitched. We note that sample C experienced local film peeling after crystallization of the SBT film. Therefore, the measurements obtained using sample C were imprecise; they are excluded from the following discussion.

To obtain further insight into the mechanism of the performance of the large memory windows exhibited in the Pt/SBT/HfO2/Si structures, we obtained a cross-sectional high-resolution transmission electron microscopy (HRTEM) image of sample A. Figure 4a indicates that sharp boundaries existed between the SBT, the HfO2 layer, and the Si substrate. The HfO2 layer exhibited a polycrystalline structure. Structural analysis through electron beam diffraction indicated the coexistence of monoclinic and tetragonal phases, with a slight amount of a residual amorphous structure, in the HfO2. In addition, an interfacial layer (IL) having a thickness of 3.5 nm was formed between the HfO2 and the Si substrate. The thickness of this IL remained almost unchanged before (not shown here) and after postdeposition annealing of the SBT. This finding suggests that the SBT deposition and crystallization (750°C, 1 min) processes had only minor influences on the IL characteristics and that such a thin
HfO₂ layer could provide a sufficiently strong barrier for this MFIS process. Using the capacitances recorded at the accumulation region, the dielectric constants calculated for the IL, HfO₂, and SBT were ca. 5.7, 20.5, and 80, respectively. The dielectric constants of the IL and HfO₂ were extracted from the Pt/HfO₂/IL/Si structure as a function of the HfO₂ thickness. The thicknesses of the HfO₂ and IL layers were all identified through TEM analysis. The capacitances of these specimens were then measured and plotted as a function of the HfO₂ thickness. The dielectric constants of the IL and HfO₂ layers (ca. 5.7 and 20.5, respectively) were extracted through linear fitting. Based on these results, the dielectric constant of SBT (ca. 80) was calculated from the Pt/SBT/HfO₂/IL/Si structure. Therefore, we could obtain the individual effective voltages of the SBT, HfO₂, and IL, which are governed by the following relationship

\[
V_i = \frac{V_f}{C_i(1/C_{\text{ferro}} + 1/C_{\text{HfO2}} + 1/C_{\text{IL}})}
\]

where \(V_i\) and \(C_i\) are the effective voltage and capacitance of the \(i\)th layer, respectively, \(V_f\) is the voltage applied to the MFIS structure, and \(C_{\text{ferro}}, C_{\text{HfO2}},\) and \(C_{\text{IL}}\) are the capacitances of SBT, HfO₂, and the IL, respectively. Using this equation, we roughly extracted the effective voltages of each layer as a function of the dielectric constant and the thickness. The estimated effective voltage applied to the SBT was as high as 0.76 \(V_f\); meanwhile, those across the HfO₂ and IL were 0.05 \(V_f\) and 0.19 \(V_f\), respectively. Therefore, the effective voltage across the SBT was 3 V when a potential of 4 V was applied; this value is two times greater than the coercive voltage (\(V_c = \text{ca. } 1.5 \text{ V in the Pt/SBT/Pt structure}\)). It is reasonable that sample A would reach a saturated memory window when \(V_f\) was larger than 4 \(V_f\), as indicated in Fig. 3b. The electric field in the IL is nearly four times greater than that in the HfO₂. The magnitude of charge injection is enhanced by a high electric field, and the memory window is narrowed upon increasing the degree of charge injection.⁵⁸ Our results suggest that the characteristics of the IL, as well as the HfO₂ buffer layer, are very important for obtaining a large memory window in MFIS structures. Although we could attribute the large memory windows to the high quality of the HfO₂, the influence from the SBT film characteristics must also be taken into consideration. Because the SBT was crystallized through RTA at 750°C within a short duration (1 min), the average grain size was relatively small. It is known that ferroelectrics with small grain sizes exhibit high \(V_c\) values; in MFIS structures, a large value of \(V_c\) results in a large memory window (i.e., the value of \(V_c\) determines the size of the memory window to a great extent).⁶

Figure 4b displays the HRTEM image of sample B, which had a Pt/SrBi₂Ta₂O₉/BL/Si MFIS structure. The SiO₂ layer grew from a thickness of 2.0 nm to ca. 5.0 nm after SBT crystallization at 750°C for 1 min. Relative to the HfO₂ sample, it has a gray layer between the SBT and SiO₂ and the interface was much rougher. Furthermore, its equivalent oxide thickness (EOT), ca. 5.0 nm was much larger than that of HfO₂/IL (EOT ca. ~3.1 nm), although the physical thickness of the HfO₂/IL was ca. 6.7 nm. Using Eq. 1, we estimated the effective voltages applied to the SBT and SiO₂ to be 0.67 \(V_f\) and 0.33 \(V_f\), respectively. Even though the effective voltage of SBT was lower (relative to that of HfO₂), the effective voltage across the SBT (4 V) was still larger than the coercive voltage of SBT films, under an applied potential of 6 V. Based on these measurements, voltages as large as 6 V may have the potential to trigger the ferroelectric domain reversion and display a wide memory window. This finding conflicts with the analytical results. Therefore, some other factors must exist that affect the characteristics of the memory window in this MFIS structure. Figure 5 displays secondary ion mass spectrometry (SIMS) depth profiles of the MFIS structures. Figure 5a indicates that the HfO₂ buffer layer in the Pt/SBT/HfO₂/Si structure inhibited the inner diffusion of SBT species effectively. Nevertheless, we clearly observed that Si atoms diffused from the substrate into the SBT layer. This phenomenon was more serious in the Pt/SBT/SiO₂/Si structure (Fig. 5b), especially near the SBT/SiO₂ interface (indicated by the circles). The SiO₂ substrate or the abundant amount of out-diffused Si possibly reacted with the SBT to form a silicate layer between the SBT and SiO₂ phases. If this situation is true, the gray layer as shown in Fig. 4b could be attributed to this silicate layer. Such a process not only brought about a rougher interface (corresponding well with the TEM image in Fig. 4b) but also created more defects within the MFIS structure; as a result, more charge-trapping centers were built, which narrowed the size of the memory window.

In conclusion, HfO₂, SiO₂, and Si₃N₄ were employed as individual insulating layers to fabricate the MFIS capacitors having Pt/SrBi₂Ta₂O₉/BL/Si structures. By using HfO₂ as the buffer layer, the Pt/SrBi₂Ta₂O₉/BL/Si structures exhibited large memory windows and high memory ratios. This enhanced performance possibly arose from the SBT characteristics and the high quality of the HfO₂ layer (high \(V_c\) value and good interfacial characteristics on the Si substrate). Such high memory ratios at low applied voltages are potentially valuable characteristics for the utilization of MFIS systems in memory applications requiring low operating potentials and low power consumption. In addition, this study also suggests that neither SiO₂ nor Si₃N₄ provide sufficiently good characteristics for their application in MFIS memories.

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