Mechanism and lifetime prediction method for hot-carrier-induced degradation in lateral diffused metal-oxide-semiconductor transistors

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The mechanism of hot-carrier-induced degradation in n-type lateral diffused metal-oxide-semiconductor (LDMOS) transistors is investigated. Experimental data reveal that hot-electron injection induced interface state generation in channel region is the main degradation mechanism. Since gate current \(I_g\) consists mainly of electron injection, \(I_g\) correlates well with device degradation. As a result, a lifetime prediction method based on \(I_g\) is presented for the purpose of projecting hot-carrier lifetime in LDMOS transistors. © 2008 American Institute of Physics. [DOI: 10.1063/1.2947588]

Lateral diffused metal-oxide-semiconductor (LDMOS) transistors have been widely used in many integrated smart-power applications because of their compatibility with standard complementary metal-oxide-semiconductor (CMOS) process. Because LDMOS devices are usually operated under high voltages, hot-carrier-induced degradation may become a serious reliability concern. To achieve a wide variety of high-voltage applications, LDMOS devices differ in device design significantly. Thus, hot-carrier-induced degradation in LDMOS transistors is more complicated than that in low-voltage metal-oxide-semiconductor field-effect transistors (MOSFETs). Several papers have reported that the degradation behavior in LDMOS transistors is quite different from that in MOSFETs.1–3 To evaluate hot-carrier reliability of the device, it is crucial to identify the degradation mechanism and predict hot-carrier lifetime of the device. In this letter, hot-carrier-induced degradation in n-type LDMOS transistors is investigated. Experimental results reveal that device degradation is induced by interface state \(N_i\) generation resulting from hot-electron injection in channel region. In addition, gate current \(I_g\) correlates well with device degradation. Finally, a lifetime prediction method based on \(I_g\) is presented for the purpose of projecting hot-carrier lifetime in our LDMOS devices.

The schematic cross section of the n-type LDMOS transistor used in this letter is shown in Fig. 1. This device is fabricated with a modified 0.25 μm CMOS process and features a n− drift region near the drain. The channel region \(L_{ch}\) and drift region \(L_{dr}\) are indicated in the figure. \(L_{ch}\) is about 0.5 μm and \(L_{dr}\) is roughly 0.7 μm. The gate oxide thickness and width of the device are 30 nm and 20 μm, respectively. The operational voltage of the device is 12 V for both drain voltage \(V_{ds}\) and gate voltage \(V_{gs}\). dc stressing under \(V_{ds}=13.2\) V and various \(V_{gs}\) (6, 9, and 12 V) is performed at room temperature. To evaluate hot-carrier-induced interface state generation \(\Delta N_i\), charge pumping technique similar to the method proposed in Ref. 6 is carried out during stressing. The stress tests are interrupted periodically to measure the degradation of device parameters [including on-resistance \(R_{on}\) and maximum transconductance \(G_{m,\text{max}}\)] and charge pumping current \(I_{cp}\). \(R_{on}\) is measured under \(V_{ds}=0.1\) V and \(V_{gs}=12\) V, while \(G_{m,\text{max}}\) is extracted under \(V_{ds}=0.1\) V.

Figure 2 shows substrate current \(I_{sub}\) and \(I_g\) as a function of \(V_{gs}\) for the device biased at \(V_{ds}=13.2\) V. Only one \(I_{sub}\) maximum occurs at \(V_{gs}=V_{ds}/2\), which is similar to the behavior in MOSFETs. \(I_g\) increases monotonically and its maximum occurs at \(V_{gs}=12\) V, indicating that more electrons are injected into gate as \(V_{gs}\) increases. In Fig. 3, \(R_{on}\) and \(G_{m,\text{max}}\) degradation as a function of \(V_{gs}\) during stressing (6, 9, and 12 V) are examined for devices stressed under \(V_{ds}=13.2\) V for 3000 s and two observations are found. First, the device stressed under higher \(V_{gs}\) produces greater device degradation. This trend is different from that in MOSFETs, where hot-carrier-induced degradation is closely related to \(I_{sub}\) and the device with larger \(I_{sub}\) is expected to produce greater device degradation.4–10 However, data in Fig. 3 show that the \(V_{gs}\) to produce the most device degradation \(V_{gs}=12\) V) matches with the \(V_{gs}\) to produce \(I_g\) maximum rather than the \(V_{gs}\) to produce \(I_{sub}\) maximum. Such a result suggests that \(I_g\) is a potential monitor to judge the severity of device degradation. Second, under the same \(V_{gs}\) during stressing, \(G_{m,\text{max}}\) degradation is much greater than \(R_{on}\) degradation. Such a result reveals that hot-carrier-induced damage is mainly located in channel region rather than n− drift region since \(G_{m,\text{max}}\) degradation is attributed to the decrease in channel mobility caused by \(\Delta N_i\) in Si/SiO2 interface.7

To evaluate hot-carrier-induced \(\Delta N_i\) in our LDMOS transistors, charge pumping measurement is performed. The

\[ \Delta N_i = \frac{\int I_{cp} \, dV_{gs}}{V_{gs}} \]

FIG. 1. (Color online) Schematic cross section of the n-type LDMOS device used in this letter. The channel region \(L_{ch}\) and drift region \(L_{dr}\) are indicated in the figure.
pulse with a fixed high level (V_b) and a variable base level (V_g) at a frequency of 500 kHz is applied to the gate. From technology computer-aided-design simulation results (under V_d=0 V), flatband voltage (V_fb), and threshold voltage (V_th) along Si/SiO2 interface can be extracted. V_fb is from 0.3 to −1 V in L_{ch} region and from −1 to −2.5 V in L_{dr} region. V_th is from 1.9 to 0 V in L_{ch} region and from 0 to −1 V in L_{dr} region. As a result, ∆N_{it} located in channel region can be sensed when V_g=4 V and V_b is varied from −1 to 3.5 V. ∆N_{it} in drift region can be sensed when V_b=0 V and V_g is varied from −3 to −0.5 V. Thus, ∆N_{it} can be extracted from charge pumping data by

$$\Delta N_{it} = \frac{\Delta I_{cp}}{qWL_{cp}},$$  

(1)

where \(\Delta I_{cp}\) is hot-carrier-induced increase in charge pumping current, \(f\) is the frequency of gate pulse, \(W\) is polygate width, and \(L_{cp}\) is the length of region where interface states are probed, i.e., L_{ch} or L_{dr}. The extracted \(\Delta N_{it}\) data reveal that \(\Delta N_{it}\) is significant in channel region, while \(\Delta N_{it}\) is small in drift region. Such a result is consistent with data analysis in Fig. 3 that hot-carrier-induced damage is mainly located in channel region. Figure 4 shows \(R_{on}\) and \(G_{max}\) degradation as a function of \(\Delta N_{it}\) in channel region for the devices in Fig. 3. ∆N_{it} correlates well with device degradation.

For LDMOS devices, \(R_{on}\) is a critical device parameter in terms of device performance. To evaluate the reliability of the device, finding a prediction method to project \(R_{on}\) lifetime (\(\tau\)) is necessary. Since the degradation mechanism in our LDMOS device is hot-electron injection in channel region and \(I_g\) consists mainly of electron injection, it is intuitive to infer that \(I_g\) correlates well with device lifetime. To confirm the above argument, Fig. 5 shows \((\tau\times I_d)\) as a function of \((I_g/I_d)\) for devices with various \(L_{ch}\) and \(L_{dr}\) (\(L_{ch} = 0.5–0.7 \mu m\) and \(L_{dr} = 0.6–1.0 \mu m\)) under different stress conditions (V_{gs}=13.2 V, V_{gs}=6 and 12 V). \(\tau\) is defined as the time needed to reach 10% of \(R_{on}\) degradation using power-law extrapolation. As seen in Fig. 5, data can be fitted to a straight line with a slope of −1.26 for both stressing V_{gs}. Such a result can be further analyzed by the following quantitative analysis. Using a procedure similar to the model for hot-electron effects proposed by Hu et al., the following three equations can be obtained:

$$I_g = C_1 I_d e^{-\phi_{it}/qE_m},$$  

(2)

$$\tau = C_2 \frac{W}{I_d} e^{\phi_{it}/qE_m},$$  

(3)

$$\frac{\tau I_d}{W} = C_3 \left(\frac{I_d}{I_{ch}}\right)^{-\phi_{it}/\phi_{ig}},$$  

(4)

where \(C_1\), \(C_2\), and \(C_3\) are technology-dependent parameters, \(\phi_{it}\) is the energy required to create gate current, \(\phi_{it}\) is the energy needed to create interface state, \(\lambda\) is hot-electron mean-free path, and \(E_m\) is the maximum channel electric field. From Eq. (4), the physical meaning of the slope in Fig. 5 is \(-\phi_{it}/\phi_{ig}\). Using \(\phi_{ig}=3.1 eV\) (the barrier height for elec-
trons to be injected to gate oxide and the slope in Fig. 5, one can derive $\varphi_{it}=3.1 \text{ eV} \times 1.26=3.9 \text{ eV}$, which is close to the value (3.7 eV) obtained by Hu et al.\textsuperscript{10} Such a quantitative agreement confirms that $\Delta N_{it}$ created by hot-electron injection in channel region is the major degradation mechanism in our device. In addition, Eq. (4) can be used to predict hot-carrier lifetime of the device.

In this letter, the mechanism and lifetime prediction method for hot-carrier-induced degradation in LDMOS transistors are discussed. Experimental results indicate that hot-electron injection induced $N_{it}$ generation in channel region is responsible for device degradation. Since $I_g$ consists mainly of electron injection, $I_g$ correlates well with device degradation. Finally, a lifetime prediction method based on $I_g$ is presented. Such a method is useful in projecting hot-carrier lifetime of LDMOS devices.