Impact of the strained SiGe source/drain on hot carrier reliability for 45 nm p-type metal-oxide-semiconductor field-effect transistors


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In this letter, the impact of the uniaxial strain SiGe source/drain (S/D) on hot carrier reliability in 45 nm p-type metal-oxide-semiconductor field-effect transistor is investigated in detail. We find that the extra mechanical stress deteriorates the gate oxide and generates interface states significantly, resulting in the hot carrier degradation dominantly driven by the drain avalanche hot carrier stress ($V_g = V_d/2$), as opposed to the channel hot electron stress ($V_g = V_d$), the well-known dominant mechanism for hot carrier degradation in the conventional deep submicron devices. A model to explain the mechanism of these observations is proposed. © 2008 American Institute of Physics.

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As the gate-oxide thickness in the complementary metal-oxide-semiconductor (CMOS) technology continues to scale down, it becomes inevitably more vulnerable under a high electric field. Consequently, the gate oxide and oxide-silicon interface are deteriorated significantly after hot carrier stress (HCS). For conventional deep submicron devices, the dominant mechanism of device degradation under HCS changes from the drain avalanche hot carriers (DAHC) injection at the maximum substrate current $I_{sub}$ ($V_g = V_d/2$) (Ref. 1) to the channel hot electron injection (CHE) under the maximum gate voltage ($V_g = V_d$). On the other hand, the strain engineering such as the embedded SiGe source/drain (S/D) has been extensively utilized to improve p-type MOS field-effect transistor (p-MOSFET) carrier mobility and implemented widely in today’s state-of-the-art p-MOSFET fabrication. For the deep nanodevices, it is highly suspected that the extra mechanical stress from strain engineering would further deteriorate gate oxide and/or interface and the strain effect would intensify the HCS degradations. However, so far, no clear studies about the influence of the mechanical stress on HCS reliability characterization have been reported. In the past, for p-MOSFETs, most of studies have been focused on the negative bias instability and been neglected for the HCS reliability because the mean free path of holes in silicon is shorter than that of the electrons and holes scatter more frequently and fewer holes could gain enough energy (about 4 eV) to deteriorate the interface and/or gate dielectric. Nevertheless, as p-MOSFET device is scaled down to deep nanoregime, both HCS reliability and the influence of a mechanical stress could not be ignored for its very small dimension.

In this letter, we report the impact of the uniaxial strain SiGe S/D on the HCS reliability in 45 nm p-MOSFETs. Experimental results show that the extra mechanical stress from the SiGe S/D would cause more serious degradations after the DAHC type stress than that after CHE type stress, a fact that is contrary to the conventional deep submicron device without strained SiGe S/D.

The p-MOSFET devices with width/length ratio of 10/0.1 were fabricated by a state-of-the-art 45 nm CMOS foundry technology on (100) silicon substrates. After shallow trench isolation and gate formation, the in situ boron doped $p^+$ Si$_{0.8}$Ge$_{0.2}$ S/D with boron concentration of $10^{18} - 10^{19}$ cm$^{-3}$ is selectively deposited under ultravacuum at 600 °C. The gate is boron doped $p^+$ polysilicon with a 1.6–1.7 nm nitride oxide grown by a decoupled plasma nitridation. In order to protect the gate damages from the SiGe S/D recess etching, before etching, we deposit a tetraethylorthosilicate film and a nitride film as the hard mask (HM). Then the HM is removed after SiGe deposition. The transmission electron microscopy examination shows intact S/D junction and no damages induced by the S/D recess etching. Subsequently, processes of lightly-doped drain implant, spacer formation, postimplantation rapid thermal annealing (RTA) (at 900 °C for 30 s), and back-end process were implemented to complete the devices. With the RTA, the damages induced by the recessing S/D etching can be reduced to a minimum. For comparison purposes, devices without SiGe S/D are also fabricated under the same processing conditions.

The HCS degradations were investigated by the widely used charge pumping (CP) method. Both DAHC and CHE stress modes are investigated. The devices were stressed under $V_g = V_d = -2$ V and $V_g = 1/2V_d = -1$ V for the CHE and the DAHC modes, respectively. In both stress modes, the source/substrate was grounded and the drain was connected to $V_d$. The stress time was set to 500 and 5000 s. The CP measurements were performed using a pulse generator (Agilent-8110) and a precision semiconductor parameter analyzer (Agilent-4156C) under the conditions of 1.5 V gate pulse, 1 MHz frequency, −0.1 V reverse bias S/D, and 80 ns of pulse rise/fall time, respectively.

Figure 1 illustrates the schematic cross section of our 45 nm p-MOSFET device with strained SiGe S/D. In general, there are some sources to deteriorate the ultrathin gate
dielectric and interface for the interface states ($N_d$) generation. One is the compressively mechanical stress resulted from the lattice mismatch between Si and SiGe ($\delta_{Si} = 5.43095 \, \text{Å}$, $\delta_{SiGe} = 5.4806 \, \text{Å}$). The mechanical stress in the channel decreases with the distance from the SiGe drain and has a maximum value located at the drain side, as shown in Fig. 2, the T-CAD (Technology Computer Aided Design pack-

![FIG. 1. (Color online) The schematic cross section of a p-MOSFET with strained SiGe S/D illustrates the different mechanisms between DAHC and CHE stress modes and the defects generated by the SiGe S/D compressive stress. The defects are marked by “XX,” where I is lightly damaged region, II is averagely damaged region, and III is heavily damaged region. The bottom left inset lists the table for comparison of the stress times under the DAHC stress.](image1)

![FIG. 2. (Color online) T-CAD simulated compressive stress contour of a 45 nm p-MOSFET with strained SiGe S/D (a) the cross section and (b) lateral distribution in channel.](image2)

![FIG. 3. (Color online) The charge pumping current ($I_{CP}$) of p-MOSFETs with and without strained SiGe S/D as a function of gate voltage ($V_g$) with different stress times under the DAHC stress mode. The inset on the right compares the normalized $I_{CP}$ of the p-MOSFETs with strained SiGe S/D after various DAHC stress time. The shift in positive $V_g$ after the DAHC stress is proportional to the stress time.](image3)
compares the normalized different stress time under the CHE stress mode. The inset on the right after various CHE stress time. The increase of SiGe mechanical stress, as illustrated in the inset of top left 133504-3 Cheng et al.

.../H92049 for DAHC and CHE stress modes, respectively. the table inserted in Fig.1, where the "increasing" and "decreasing" for the amount after the
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cally reduced. Thus, its effect on hot carrier degradation be-
will induce S/D leakage; however, in this work, due to the
degradations. Conventionally, this etching-induced damage
effects may contribute to the hot carrier
S/D. Furthermore, other source such as the recessing S/D
etching-induced damages may contribute to the hot carrier
degradations. Conventional, this etching-induced damage
will induce S/D leakage; however, in this work, due to the
addition of hard mask and RTA, the damages are dramatically reduced. Thus, its effect on hot carrier degradation becomes minor, as compared to the SiGe mechanical stress and high electric field resulted from the HCS.

We also compare the threshold voltage shifts (ΔVth), saturation current degradations (ΔIdsat), and number of interface states (Nit) in both SiGe and non-SiGe devices after 5000 s for DAHC and CHE stress modes, respectively. (Please see the table inserted in Fig. 1, where the “+” and “−” means the “increasing” and “decreasing” for the amount after the stress from the initial value, respectively.) In the non-SiGe devices, the increasing of Nit number after CHE mode stress (44.54%) is larger than that after DAHC stress (5.53%), suggesting that the CHE mode dominates the HCS degradation, a well-known phenomena in the deep submicron devices.

However, in the SiGe devices, Nit after DAHC stress mode increases substantially to 945.12%, much larger than 57.8% after CHE stress mode. Similar observation is found on the ΔVth and Idsat degradations as well. Clearly, the dominant mechanism of HCS degradation is the DAHC stress mode in the presence of strained SiGe S/D.

In summary, the HCS degradations in 45 nm p-MOSFETs with and without uniaxial strain SiGe S/D have been investigated and compared. The strained SiGe S/D significantly enhances the hot carrier damages at the interface and gate oxide, especially near to the drain. Consequently, the dominant mechanism of HCS degradation in the strained SiGe S/D devices is found to be different from that in non-strained devices. Thus, it is suggested the influence of mechanical stress on HCS degradation could be more severe in the advanced deep nano devices for the further dimension scaling.

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