Characteristics Improvement for an n–p–n Heterostructure Optoelectronic Switch by Introducing a Wide-Gap Layer in the Collector

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In order to achieve high optical sensitivity and low holding power, a wide-gap carrier confinement layer was introduced into the collector region of an n-p-n-heterostructure optoelectronic switch. A similar device without the confinement layer was also fabricated to demonstrate the performance improvement. Both devices were found to have bistable electrical states: a high-impedance OFF state connected to a low-impedance ON state by a region of negative differential resistance. The functional characteristics were based on avalanche multiplication.

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The optoelectronic switch is a device with two distinct stable states, i.e., a high-impedance OFF and a low-impedance ON state. Switching from one state to the other can be induced by either optical or electrical input. In two-dimensional arrays for parallel optical information processing, the optoelectronic switch is a primary device. To avoid the excess heat dissipation, low holding power is required in the characteristics of the device. To achieve the high optical fanout, high light output and high optical sensitivity are also essential. Because the light output is limited by the heat dissipation, improving the optical sensitivity is optimized. With high gains and high-speed operations, n-p-n heterostructures can be used to produce promising optoelectronic switches. In this work, n-p-n heterostructures are exploited as optoelectronic switches. To improve the device performance, a wide-gap carrier confinement layer is introduced into the collector region of one of the studied devices. The device with the confinement layer presents a lower holding power and a higher optical sensitivity than the one without the confinement layer.

The structure of the device with a confinement layer in the collector region, numbered device G220, consisted of a 300 nm n + -GaAs (3 × 10^{10} cm^{-3}) buffer layer, a 200 nm n-i-GaAs layer, a 50 nm N-Al_{0.4}Ga_{0.6}As (8 × 10^{11} cm^{-3}) confinement layer, a 50 nm n-GaAs (8 × 10^{13} cm^{-3}) layer, an 80 nm p + -GaAs (8 × 10^{18} cm^{-3}) layer, a 200 nm N-Al_{0.4}Ga_{0.6}As (5 × 10^{15} cm^{-3}) layer, and a 200 nm n + -GaAs (3 × 10^{18} cm^{-3}) cap layer. The structure of the device without the confinement layer, numbered device G330, was the same as that of device G220 except that the 50 nm N-Al_{0.4}Ga_{0.6}As (8 × 10^{13} cm^{-3}) confinement layer was replaced by a 50 nm n-GaAs (8 × 10^{17} cm^{-3}) layer. The devices were grown by molecular beam epitaxy (MBE) on (100)-oriented n-GaAs substrates. The growth rate of the GaAs host material was 1.0 μm/h. Si and Be were used as n- and p-type dopants, respectively. The growth temperature of the GaAs material was 580°C. After finishing the growths, circular mesas, 70 μm in diameter, were made by etching down to the substrates for both devices. The mesa etchings were finished by employing NH_{4}OH/H_{2}O_{2}/H_{2}O solution. The contacts to the cap layers of the mesas were made using the evaporation and liftoff of AuGe in the form of a ring, which was enlarged on one side to enable bonding. The open areas for the optical windows had a diameter of 30 μm. AuGe was also used as the ohmic contact metal to the substrates. Figure 1 shows the cross-sectional view of devices G220 and G330.

For an n-p-n structure under a positive collector-to-emitter (C–E) voltage V_{CE} with base (B) open, the collector current I_{C} is approximated to

\[ I_{C} = \frac{M I_{CO}}{1 - \alpha M} \]

where

\[ M = \frac{1}{1 - \left(\frac{V_{CB}}{B V_{CBO}}\right)^{n}} \]

I_{CO} is the collector reverse saturation current including the base–collector (B–C) junction leakage current and photocurrent, α the common-base current gain, M the avalanche multiplication factor, B V_{CBO} the B–C breakdown voltage with emitter open, V_{CE} the external voltage drop across the B–C junction, and n a constant which...

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**Figure 1.** Cross-sectional view of devices G220 and G330. The structure of device G330 is the same as that of device G220 except that the 50 nm N-Al_{0.4}Ga_{0.6}As (8 × 10^{17} cm^{-3}) layer is replaced by a 50 nm n-GaAs (8 × 10^{17} cm^{-3}) layer.
is about 3.5 for GaAs. The switching performance in an n-p-n structure operating in the avalanche region is produced by the positive feedback between the avalanche multiplication in the B–C junction and the current gain given by the transistor action. According to Eq. 2, $M$ increases with a positive $V_{CE}$ voltage, because the reverse-biased B–C junction absorbs most of the voltage. The multiplied holes generated in the B–C junction move toward the base, charge the E–B junction, and then reduce the E–B potential. More electrons are therefore injected from the emitter into the base and reach the B–C junction, which generates more electron-hole pairs. This process is the so-called “positive feedback loop.” For the $V_{CE}$ voltage large enough to turn $1 - \alpha M$ to zero, the B–C junction could break down, according to Eq. 1. From Eq. 2, the $1 - \alpha M = 0$ condition can define a switching voltage $V_S$ as

$$V_S = B V_{CBO} \left(1 - \alpha \right)^{1/\alpha} \quad [3]$$

If $\alpha$ increases with $I_c$ after $V_{CE} = V_p$, the criterion for the B–C breakdown will conduct a reduction in $M$ for $M = 1/\alpha$. This $M$ reduction requires a smaller B–C voltage. As a consequence, a negative-differential-resistance (NDR) phenomenon is expected in the breakdown characteristics. Then, a low-impedance ON state is obtained if $\alpha$ saturates.

Figure 2 shows the band diagrams of devices G220 (solid lines) and G330 (dotted lines) under a positive $V_{CE}$ voltage. The holes photogenerated in the n+GaAs layers on both sides of the devices could be neglected, as those holes are recombined in the dense surrounding electron gas. In the emitter region, the photogenerated electrons transport toward the base, and holes move in opposite direction for the forward biasing in the E–B junction. In the base and collector regions, the photogenerated electron-hole pairs are separated by the existing electric field. The photogenerated holes move down to well A, and then are confined in well A or charge the E–B junction, as shown in Fig. 2. Due to the presence of the E–B valence-band discontinuity, the holes in well A experience more effective confinement. The photogenerated electrons move toward the substrate. For device G220, part of the electrons are confined in well B, as shown in Fig. 2, due to the existence of the wide-gap AlGaAs layer in the collector region, and others are collected by the electrode. The holes charging the E–B junction and the holes confined in well A lower the potential barrier of the base for both devices. If the $V_{CE}$ voltage is high enough, the breakdown occurs in the 200 nm i-GaAs layer in the collector region. The multiplied holes are also confined in well A or charge the E–B junction to lower the barrier, and then the electrons emitted over the barrier from the emitter to the base are increased. This positive feedback process results in an S-shaped NDR performance in the current–voltage $I$–$V$ characteristics of both devices. Because the characteristics of both devices are influenced by the input-light power, the switching is controllable by changing the input light. Because the photogenerated electrons confined in well B increase the voltage drop across the 200 nm i-GaAs layer in the collector region, the switching characteristics of device G220 exhibit a higher optical sensitivity and a lower holding power than that of device G330, which are discussed in the following paragraphs.

The experimental $I$–$V$ curves of devices G220 and G330 under dark and illumination at 300 K are shown in Fig. 3 and 4, respectively.
The higher optical sensitivity of device G220 is due to the breakdown. Thus, the switching voltage $V_S$ of device G220 is smaller than that of device G330. Consequently, a lower holding power $P_H = I_H \times V_H$ is obtained in the G220 characteristics.

In summary, we have reported about the enhancement in optical sensitivity and the decrement in holding power of an n–p–n optoelectronic switch by introducing a wide-gap confinement layer into the collector region. The performance improvement can result in a lower power consumption and larger fanin-to-fanout ratio, which are very useful for the design and fabrication of optical parallel processing.

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**References**