The effects of nitrogen concentration on the thermal stability and electric properties of the WN film as the gate electrode are investigated. WN is deposited by using reactive radio frequency sputtering, and films with composition of WN$_{0.6}$, WN$_{0.8}$, and WN$_{1.5}$ are obtained at 10, 25, and 40% of N$_2$ partial flow ratio, respectively. The crystal structure of the WN$_{0.6}$ film indicates that this film is a mixture of W + W$_2$N, while WN$_{0.8}$ and WN$_{1.5}$ films both show the W$_6$N phase. After annealing in N$_2$ + H$_2$ (N$_2$/H$_2$ = 9:1) ambient at 500°C, the surface of the WN$_{0.6}$ film reveals only the W–O bonding but no W–N bonding. In addition, oxygen diffuses from SiO$_2$ into WN$_{0.6}$ and leads to the formation of a mixing layer. Subsequently, flatband voltage ($V_{FB}$) of the metal oxide semiconductor capacitor shifts positively after annealing at 500°C. After annealing at 500°C, WN$_{0.8}$ and WN$_{1.5}$ films exhibit better resistance to oxidation than the WN$_{0.6}$ film, regardless of the surface of the WN$_{0.6}$ film or the interface between WN$_{0.6}$ and SiO$_2$. Resistivity of all WN films increases after annealing and also increases with increasing nitrogen content in the WN films. However, neither the nitrogen content in the WN$_{0.6}$ nor the postmetal annealing affect the leakage current of WN$_{0.6}$/SiO$_2$/Si capacitors at both positive and negative biases.

Influence of Nitrogen Content in WN$_x$ on Its Thermal Stability and Electrical Property as a Gate Electrode

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The dimension of complementary metal oxide semiconductor (CMOS) devices shrinks continuously in order to improve the electrical performance. At the same time, the choice of the gate electrode materials becomes an important issue. The conventional polysilicon gate electrode of CMOS devices suffers several problems, such as gate depletion and boron penetration into the channel region.1–4 Gate depletion decreases the capacitance of the device and degrades the driving capability of the channel current.1,2 Boron penetration in the p-channel metal oxide semiconductor field effect transistor (PMOSFET) reduces the control of threshold voltage and gate oxide reliability.3,4 Therefore, metals or metal nitrides are interesting materials for gate electrode applications. Gate electrode work functions, resistivity, and compatibility with CMOS technology are key parameters.5 Nitrogen-implanted Mo (Ref. 6) and thin films of Ti$_{1-x}$Al$_x$N$_y$,7 Ta–Pt,8 Ta–Ti,8 and Ti–Ni (Ref. 9) have been investigated as gate electrodes. By varying their atomic composition, these materials may possess a suitable work function for gate-electrode applications. The thermal stability of TiN$_{0.9}$–10 WN$_{1.3}$, TaN$_{1.3}$, TaSi$_{1–x}$Ni$_x$,17 and WSi$_2$ (Ref. 18) has been discussed to see their compatibility with the gate-electrode process. Unfortunately, metal nitrides generally exhibit high resistivity. However, resistivity of gate electrodes can be reduced by the stacking structure, such as W/TiN,19,20 W/WN$_x$,21 and Ta/TaN$_x$.22

Therefore, the literature suggests that metal nitrides are approved materials for gate electrodes. Nevertheless, the nitrogen concentration and structure of metal nitride gate electrodes are not fully explored in previous studies. In this study, WN$_x$ and SiO$_2$ are chosen as the gate electrode and gate dielectric of MOS capacitors, respectively. The WN$_x$ represents three W–nitride films of different nitrogen content. Thermal stability and electrical properties of WN$_x$/SiO$_2$/Si MOS capacitors are investigated after prolonging (30 min) postmetal annealing at 400–600°C in N$_2$ + H$_2$ ambient. The phase and microstructure, compositional depth profiles, and chemical bonding states of the WN$_x$ electrode as well as the WN$_x$/SiO$_2$ interface after postmetal annealing are investigated. The connection between material characteristics and the electrical performance of WN$_x$/SiO$_2$/Si MOS capacitors is also discussed.

Experimental

The substrate used in this study was an n-type Si(100) wafer with a resistivity of 1–10 Ω cm. The silicon wafer was cleaned in organic baths and chemically etched with diluted hydrofluoric acid (HF) solution, followed by thermal oxidation in a quartz tube furnace at 1050°C. The thickness of the resulting SiO$_2$ films was determined by a spectroscopic ellipsometer and the value was 25 nm. The WN$_x$ film was then deposited on the SiO$_2$ layer by reactive magnetron sputtering using a W target (2 in. diam, 99.9% purity). The base pressure of the chamber was 3 × 10$^{-6}$ Torr and the working pressure was 7 mTorr. The total gas (Ar + N$_2$) flow rate was kept at 100 sccm and the N$_2$ partial flow rate (the ratio of N$_2$ flow rate to total flow rate) was set at 10, 25, and 40% to fabricate WN$_x$ films of three different compositions. The radio frequency (rf) power supplied to the target was 150 W, and the substrate holder was neither cooled nor heated externally but applied with a negative 100–V dc bias. Depending on the N$_2$ partial flow rate, the resulting WN$_x$ film thickness varies from 160–180 nm, as examined by scanning electron microscope (SEM) on the same cross section.

After the WN$_x$/SiO$_2$/Si structure was completed, postmetal annealing was carried out in a quartz tube furnace at 400–600°C in N$_2$ + H$_2$ ambient (N$_2$ flow rate = 135 sccm and H$_2$ flow rate = 15 sccm) for 30 min to investigate the thermal stability. Atomic ratio of N/W in the films was determined by Rutherford backscattering spectrometry (RBS) with 2-MeV He$^+$ ion beams. The phase transformation after postmetal annealing was investigated by glancing incident angle X-ray diffraction (GIXRD) with Cu K$_\alpha$ radiation ($\lambda = 0.1542$ nm) and an incident angle of 2°. The microstructure of WN$_x$ and WN$_x$/SiO$_2$ interface was examined by high-resolution transmission electron microscopy (HRTEM). Auger electron spectrometry (AES) was used to characterize the distribution of elements after the postmetal annealing. Chemical bonding states of the samples were investigated using X-ray photoelectron spectroscopy (XPS) with Mg K$_\alpha$ radiation (1253.6 eV). Film resistivity was obtained from sheet resistance measured by a four-point probe. The MOS capacitors were characterized electrically using a computer-controlled HP 4284 LCR meter for hysteresis loops at a frequency of 100 kHz with a small ac signal of 25 mV. The current densities were measured by an HP 4140B pA meter/dc voltage source.

Results and Discussion

Material characteristics of WN$_x$ film on SiO$_2$, as deposited and after annealing.— The W/N ratios of WN$_x$ films are analyzed using RBS and the details were reported in our previous work.23 With 10, 25, and 40% of N$_2$ partial flow ratio during sputtering, the W/N ratios of WN$_x$ film are 1:0.6, 1:0.8, and 1:1.5, respectively. Accordingly, WN$_{0.6}$ films sputtered at 10, 25, and 40% N$_2$ partial flow ratio are referred to as WN$_{0.6}$/SiO$_2$, WN$_{0.8}$/SiO$_2$, and WN$_{1.5}$/SiO$_2$, respectively.

Figure 1a–c shows the GIXRD spectra of WN$_{0.6}$/SiO$_2$, WN$_{0.8}$/SiO$_2$, and WN$_{1.5}$/SiO$_2$.
WN$_{0.6}$ films after annealing at various temperatures, respectively. The diffraction peaks of as-deposited WN$_{0.6}$ films are associated with (111), (200), (220), and (311) diffractions of W$_2$N (ICDD PDF 25-1257) and a broad (110) body-centered cubic (bcc)-W diffraction at $2\theta \approx 40^\circ$ (ICDD PDF 04-0806) (Fig. 1a), indicating that the WN$_{0.6}$ film is a W + W$_2$N mix phase. The diffraction peaks nearby $2\theta = 40^\circ$ of as-deposited, 400°C- and 500°C-annealed WN$_{0.6}$ films (Fig. 1a) are deconvoluted and shown in Fig. 2a-c, respectively. The deconvolution indicates that the crystal structure of 400°C-and 500°C-annealed samples are still a mixture of W + W$_2$N. Neither W nor W$_2$N exhibits sharp crystallization. After annealing at 600°C (Fig. 1a), the WN$_{0.6}$ films shows improved crystallinity and the diffraction peaks are associated with W$_2$N, bcc-W, and WO$_3$ (ICDD PDF 83-0947) phases. In Fig. 1b, the diffraction peaks of as-deposited, 400°C-annealed, and 500°C-annealed WN$_{0.8}$ films are pertaining to (111), (200), (220), and (311) planes of W$_2$N, and these peaks are significant and sharp, indicating that the WN$_{0.8}$ film exhibits good crystallinity. After annealing at 600°C, additional diffraction peaks pertaining to the WO$_3$ structure are observed, but they are not as significant as those seen in the 600°C-annealed WN$_{0.6}$.

As for the X-ray diffraction (XRD) patterns of WN$_{1.5}$ films (Fig. 1c), they are similar to the patterns of WN$_{0.8}$; however, all
high-energy side doublet is associated with the W 4f 7/2 and W 4f 5/2 peaks of oxygen-bonded W. The intensity of the W 4f 7/2 and W 4f 5/2 peaks of nitrogen-bonded W increases with increasing N2 flow ratio, and oxygen-bonded W peaks of 500°C-annealed WN0.6 film are the most significant among the three. It is clear that the WN film with high nitrogen content has a better ability to prevent the oxidation after annealing than the WN film with low nitrogen content. The heats of formation for W2N and WO3 are −17 and −200 kcal/mol, respectively.24 Although the oxidation of W2N is thermodynamically favored, W atoms in a N-rich environment are more resistant to oxidation.

To further understand whether the oxidation of WN occurs only on the surface or across the whole film, we have carried out elemental depth profiling on the 500°C-annealed WN films using AES. Figure 5a-c shows the AES depth profiles of the WN0.6/SiO2/Si, WN0.8/SiO2/Si, and WN1.5/SiO2/Si samples after annealing at 500°C, respectively. It is clear that the oxidation of WN is limited on the surface and it is most significant for the WN0.6 film (Fig. 5a). In addition, Fig. 5a also indicates that oxygen diffuses from SiO2 to WN0.6 film after annealing at 500°C. In contrast, the interfaces of WN0.8/SiO2 and WN1.5/SiO2 remain sharp after annealing at 500°C (Fig. 5b and c). When comparing the AES profiles of as-deposited (not shown) and 500°C-annealed WN films, we have found that the intensities of W and N signals in the bulk of WN films (not including the oxidized regions) remain unchanged before and after annealing. Although the surface of WN films is oxidized, the composition inside WN films is stable after annealing at 500°C.

Diffusion of oxygen at the interface between WN0.6 and SiO2 is further investigated using HRTEM. Figure 6 shows the HRTEM micrograph on the WN0.6/SiO2 interface after annealing at 500°C. The micrograph indicates that a layer of different contrast and non-uniform thickness lies between WN0.6 and SiO2. This interlayer should correspond to the oxygen-diffusing layer observed in the AES depth profiles (Fig. 5a).

Electric properties of WN/SiO2/Si MOS capacitor.—To determine whether the nitrogen content in WN affects its electrical properties, we carried out resistivity and hysteresis capacitance-voltage (C–V) and current-voltage (I–V) measurements on the WN/SiO2/Si structure. Because the WN films are oxidized after annealing at 600°C, the electrical properties are measured on the samples which are required to form W–N compounds.23 The excess nitrogen atoms may exist interstitially in the lattice or locate along the grain boundaries.

Surface chemical bonding states of 500°C-annealed WN films are examined by XPS and the W 4f spectra are shown in Fig. 4. The low-energy side doublet is associated with the W 4f 7/2 and W 4f 5/2 peaks of nitrogen-bonded W and high-energy side doublet is associated with the W 4f 7/2 and W 4f 5/2 peaks of oxygen-bonded W. The peaks of W 4f 7/2 and W 4f 5/2 peaks of nitrogen-bonded W increases with increasing N2 flow ratio, and oxygen-bonded W peaks of 500°C-annealed WN0.6 film are the most significant among the three. It is clear that the WN film with high nitrogen content has a better ability to prevent the oxidation after annealing than the WN film with low nitrogen content. The heats of formation for W2N and WO3 are −17 and −200 kcal/mol, respectively.24 Although the oxidation of W2N is thermodynamically favored, W atoms in a N-rich environment are more resistant to oxidation.

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were annealed at temperatures of 500°C or lower. Resistivity values of WN\textsubscript{x} films of various compositions, as deposited and after annealing, are listed in Table I. Thicknesses of the WN\textsubscript{x} films are also listed in Table I. The thickness of the WN\textsubscript{0.6} film increases slightly with increasing annealing temperature, which is attributed to the oxidation of the WN\textsubscript{0.6} film. However, the thickness of the WN\textsubscript{0.8} and WN\textsubscript{1.5} films is independent of the annealing temperature. Resistivity of all WN\textsubscript{x} films increases after annealing, suggesting that oxidation of the WN\textsubscript{x} surface would increase the resistivity of WN\textsubscript{x} films. In addition, resistivity of WN\textsubscript{x} films also increases with increasing nitrogen content in the WN\textsubscript{x} films.

Dielectric characteristics of the WN\textsubscript{x}/SiO\textsubscript{2}/Si structure are investigated by measuring the hysteresis C–V and I–V curves. Figure 7a-c shows the high-frequency (100-kHz) hysteresis C–V curves of the as-fabricated and annealed WN\textsubscript{0.6}/SiO\textsubscript{2}/Si, WN\textsubscript{0.8}/SiO\textsubscript{2}/Si, and WN\textsubscript{1.5}/SiO\textsubscript{2}/Si capacitors, respectively. The hysteresis offset is attributed to the trapping site within the dielectric layer (SiO\textsubscript{2}). The density of charges, \(N_h\), can be calculated by the following equation:

\[
N_h = \frac{C_{ox} \Delta V_{hysteresis-off}}{qA}
\]

where \(C_{ox}\) is the capacitance of the oxide layer, \(\Delta V_{hysteresis-off}\) is the hysteresis offset of the flatband voltage, \(q\) is the electron charge, and \(A\) is the capacitor area. The values of \(\Delta V_{hysteresis-off}\) and \(N_h\) for all MOS capacitors are listed in Table II. In this study, the direction of hysteresis C–V curves is clockwise; accordingly, \(N_h\) is associated with the negative charge-trapping site. The \(N_h\) which is contributed to the trivalent silicon (\(\equiv\text{Si}\cdot\equiv\)) is located near the SiO\textsubscript{2}/Si interface\textsuperscript{26,27} and it can react with hydrogen.\textsuperscript{28} The suitable temperature of the reaction is 450°C,\textsuperscript{29} and the hydrogen may be released after annealing above 450°C. The \(N_h\) of all MOS capacitors decreases after annealing at 400°C and slightly increases as compared to the 400°C-annealed one after annealing at 500°C (Table II). Consequently, the reduction of \(N_h\) after annealing at 400°C is attributed to the decrease of trivalent silicon by reacting with hydrogen. However, the release of hydrogen is responsible for the increase of \(N_h\) after annealing at 500°C.

To further understand whether the annealing temperature affects the flatband voltage of the MOS capacitors, the relative shift of

![Figure 5. AES depth profiles of the WN\textsubscript{x}/SiO\textsubscript{2}/Si MOS structures after annealing at 500°C: (a) WN\textsubscript{0.6}/SiO\textsubscript{2}/Si, (b) WN\textsubscript{0.8}/SiO\textsubscript{2}/Si, and (c) WN\textsubscript{1.5}/SiO\textsubscript{2}/Si.](image)

![Figure 6. Cross-sectional TEM micrograph of the WN\textsubscript{0.6}/SiO\textsubscript{2}/Si sample after annealing at 500°C.](image)
We are comparing the change of flatband voltage shown as $V_{FB,annealing}$ before and after annealing between the flatband voltage of samples after annealing is also listed in Table II. The relation is:

$$V_{FB,annealing} = \Phi_{ms,annealing} - \frac{Q_{annealing}}{C_{ox}}$$

We are comparing the change of flatband voltage ($\Delta V_{FB,annealing}$) before and after annealing. Therefore, the change of flatband voltage ($\Delta V_{FB,annealing}$) before and after annealing is shown in Eq. 3.

$$\Delta V_{FB,annealing} = \Delta \Phi_{ms,annealing} - \frac{\Delta Q_{annealing}}{C_{ox}}$$

Table II. Data extracted from forward hysteresis C–V curves and hysteresis loops. $\Delta V_{hysteresis-offset}$ is the flatband voltage offset of the hysteresis loops ($V_{FB}$ of the MOS after annealing) $-$$V_{FB}$ of the as-fabricated MOS).

<table>
<thead>
<tr>
<th>Film</th>
<th>Annealing temperature (°C)</th>
<th>$\Delta V_{hysteresis-offset}$ (mV)</th>
<th>$N_d$(cm$^{-2}$)</th>
<th>$\Delta V_{FB,annealing}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>WN$_{0.6}$</td>
<td>As-fabricated</td>
<td>411</td>
<td>$3.34 \times 10^{11}$</td>
<td>1.25</td>
</tr>
<tr>
<td>400</td>
<td>4</td>
<td>3.81 $\times 10^9$</td>
<td>2.02 $\times 10^{10}$</td>
<td>2.30</td>
</tr>
<tr>
<td>500</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WN$_{0.8}$</td>
<td>As-fabricated</td>
<td>290</td>
<td>$2.99 \times 10^{11}$</td>
<td>1.70</td>
</tr>
<tr>
<td>400</td>
<td>10</td>
<td>9.71 $\times 10^8$</td>
<td>3.47 $\times 10^{10}$</td>
<td>1.21</td>
</tr>
<tr>
<td>500</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WN$_{1.5}$</td>
<td>As-fabricated</td>
<td>437</td>
<td>$3.81 \times 10^{11}$</td>
<td>2.25</td>
</tr>
<tr>
<td>400</td>
<td>3</td>
<td>2.63 $\times 10^8$</td>
<td>5.07 $\times 10^{10}$</td>
<td>1.64</td>
</tr>
<tr>
<td>500</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The $C_{ox}$ of annealed MOS structure is similar to that of as-fabricated MOS structure; therefore, $C_{ox}$ of the MOS structure, before and after annealing, can be seen as a constant.

The result of AES depth profile analysis (Fig. 5) shows that the composition of W and N inside WN$_x$ films is stable after annealing, except for 500°C-annealed WN$_{0.6}$ film. Accordingly, the work function of these annealed films is similar to that of the as-fabricated films (i.e., $\Delta \Phi_{ms,annealing} = 0$). Assuming $\Delta \Phi_{ms,annealing} = 0$ upon annealing, the change of flatband voltage ($\Delta V_{FB,annealing}$) is related to the change in the amount of oxide charges upon annealing ($\Delta Q_{annealing}$). The positive change of flatband voltage ($\Delta V_{FB,annealing} > 0$) is attributed to the decrease of positive charges or increase of negative charges. Oppositely, the negative change of flatband voltage ($\Delta V_{FB,annealing} < 0$) is attributed to the increase of positive charges or decrease of negative charges. In addition, the charges in the SiO$_2$ film are mostly positive and mainly attributed to the nonstoichiometric silicon–oxygen species ([Si–O]+$^{30-32}$). Therefore, the positive change of flatband voltage for 400°C-annealed MOS structure ($\Delta V_{FB,annealing} > 0$) shall be attributed to the decrease of the positive charges in the SiO$_2$ layer. Razouk et al. indicated that the quantity of positive oxide charges related with incompletely oxidized Si atoms in the SiO$_2$ would decrease after annealing in the inert ambient (e.g., N$_2$ or Ar) due to formation of the perfect Si–O–Si bonding network.$^{34}$

The $\Delta V_{FB,annealing}$ values of 500°C-annealed WN$_{0.8}$/SiO$_2$/Si and WN$_{1.5}$/SiO$_2$/Si structures are less than those of 400°C-annealed WN$_{0.8}$/SiO$_2$/Si and WN$_{1.5}$/SiO$_2$/Si structures. Hickmott reported that the Si and SiO$_2$ react and form gaseous SiO after annealing at 500°C and above. The gaseous SiO can diffuse into SiO$_2$; however, if SiO condenses, it can provide a positive oxide charge, which decreases $V_{FB}$ of the capacitor. Consequently, the smaller $\Delta V_{FB,annealing}$ of 500°C-annealed WN$_{0.8}$/SiO$_2$/Si and WN$_{1.5}$/SiO$_2$/Si structures is attributed to the formation of SiO, but for the WN$_{0.6}$ film, an interface layer between WN$_{0.6}$ and SiO$_2$ was formed after annealing at 500°C (see Fig. 5a and 6). This interfacial layer may induce substantial charges in oxide as well as affect the work function of WN$_{0.6}$ (i.e., the assumption of $\Delta \Phi_{ms,annealing} = 0$ is no longer proper). Therefore, the discussion on the $\Delta V_{FB,annealing}$ of the WN$_{0.8}$ and WN$_{1.5}$ systems is not appropriate for the WN$_{0.6}$ system. The exact reason for the increase of $V_{FB,annealing}$ of the 500°C-annealed WN$_{0.6}$/SiO$_2$/Si MOS capacitor, as compared with its value of the 400°C-annealed sample, is yet to be explored.

With regard to the leakage current behavior, current density for all MOS capacitors at $+1$ and $-1$ MV/cm are listed in Table III. The gate voltage ($V_g$) had been corrected to $V_g - V_{FB}$.
tering deposition of the WN, WN0.8, WN0.6, SiO2/Si capacitors, before and after annealing at 400 or 500°C, at +1 and −1 MV/cm electrical field. Some of the current density values at positive bias are labeled as <10⁻¹⁸ A/cm², which is due to the lowest leakage current (at the level of 10⁻¹⁸ A/cm²) as measured by HP4140B. 

\( V_n = V - V_{ph} \) \(^\text{35}\), and the electric field \((E)\) equals \((V - V_{ph})/(\text{oxide thickness})\). Some of the current density values at positive bias are labeled as <10⁻¹⁰ A/cm², which is due to the lowest leakage current (at the level of 10⁻¹⁰ A/cm²), as measured by HP4140B. At +1 MV/cm electrical field, the leakage current density for all MOS capacitors, except for the 500°C-annealed WN0.6/SiO2/Si structure, is lower than 10⁻⁹ A/cm², while the leakage current of 500°C-annealed WN0.6/SiO2/Si structure is slightly higher than 10⁻⁸ A/cm² (2.16 × 10⁻⁹ A/cm²) at positive bias. Under −1 MV/cm electrical field, the leakage current density of all MOS capacitors varies from 1 to 9 × 10⁻⁹ before and after annealing at 400 and 500°C. Therefore, the postmetal annealing does not affect the leakage current of WN/SiO2/Si capacitors at both positive and negative biases.

According to Table III, we also notice that the leakage current at negative bias is generally higher than that at positive bias. For the oxide layer which is under low electric field, Schottky emission is expected to dominate the leakage current of MOS structure. The barrier height (4.1 eV) of WN/SiO2 junction is larger than that (3.5 eV) of SiO2/Si junction. \(^\text{56}\) In this study, the barrier height of WN/SiO2 is calculated from the WN work function, and the work function of WN is 5.0 eV. \(^\text{37}\) Hence, if the mechanism of leakage current is mainly related to Schottky emission, the leakage current under positive bias (the electron injected from Si to SiO2) is larger than that under negative bias (the electron injected from WN to SiO2). Nevertheless, in our study, the leakage current density of WN/SiO2/Si capacitors at −1 MV/cm electrical field is higher than that measured at +1 MV/cm. This can be attributed to the irradiation damage in SiO2 (near the WN/SiO2 interface) arisen from the sputtering deposition of the WN electrode. The sputtering-induced defects enhance the electron flow from the WN electrode to the SiO2 dielectric. As a result, the negatively biased leakage current is enlarged, as shown in Table III.

### Conclusion

Dependence of the material and electrical properties of sputtered WNx gate electrode on its nitrogen content is investigated. For three WNx films of different compositions (WN0.8, WN0.6, and WN1.3), the nitrogen concentration determines their phases, crystallinity, resistance to surface oxidation, and interdiffusion at the WN/SiO2 interface. Resistivity of WNx increases with increasing nitrogen content, while C–V and I–V characteristics of WN/SiO2/Si MOS capacitors are generally in sensitive to the nitrogen concentration of Wnx. WN0.6 possesses a rather low resistivity but has poor oxidation resistance, and interdiffusion at the WN0.6/SiO2 interface upon postmetal annealing at 500°C leads to the increase of defects in the MOS structure. WN1.3 is thermally stable but exhibits a high resistivity. As a consequence, the WN0.6 film is the optimum W-nitride gate electrode for practical application in MOS devices.

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