Low leakage current Cu(Ti)/SiO₂ interconnection scheme with a self-formed TiOₓ diffusion barrier

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(Received 10 December 2001; accepted for publication 12 February 2002)

Electrical and material properties of Cu(0.02 wt % Ti) alloy and pure Cu films deposited on SiO₂/Si are explored. Current–voltage measurement using metal–oxide–semiconductor (MOS) capacitor structure reveals low leakage current (10⁻⁸ A/cm²) for capacitors with as-deposited Cu(0.02 wt % Ti) and pure Cu metal gates. However, after annealing at 700 °C in a vacuum, leakage current of MOS capacitors using a pure Cu gate shows a dramatic rise of leakage current at a low electrical field, while the leakage current of capacitors with Cu(0.02 wt % Ti) gate stays at ~10⁻⁷ A/cm². Concurrently, the resistivity of annealed Cu(0.02 wt % Ti) is reduced to 2.5 μΩ cm, which is only slightly greater than the resistivity of as-sputtered pure Cu films. X-ray photoelectron spectroscopy indicates that a TiOₓ layer has formed at the Cu(0.02 wt % Ti)/SiO₂ interface after annealing and Auger electron spectroscopy depth profiles show less interdiffusion at the Cu(0.02 wt % Ti)/SiO₂ interface than the Cu/SiO₂ interface. The correlation between leakage current reliability and the interfacial reaction upon annealing is discussed. © 2002 American Institute of Physics.

As the feature size of the ultralarge scale integration (ULSI) circuits decreases, resistance–capacitance delay of the interconnection becomes a serious factor in determining the overall delay of the circuits. Recently, copper has become the major material of the interconnect metallization because of its low resistivity (~1.7 μΩ cm for bulk) and higher electromigration resistance than the conventional Al-based interconnects.

However, copper has a few major disadvantages for application in ULSI metallizations. First of all, pure copper does not adhere well to SiO₂-based dielectrics, and it has a high diffusivity in both Si³ and SiO₂. Also, copper does not form self-passivating oxide layer in air so that it has a poor oxidation resistance.

To avoid these problems, an adhesion layer and diffusion barrier are used between copper and SiO₂ or silicon. Nevertheless, the additional layer may either complicate the processes or increase the overall resistance. An alternative approach is to alloy copper with additive atoms. It has been reported that copper alloying with a refractory metal (such as Ti and Cr) can improve the adhesion of copper, and alloying with Ti will improve electromigration resistance. In addition, Ti in a Cu–Ti alloy film will segregate to the free surface and form a stable self-passivating TiN layer after annealing at ~550 °C in an ammonia ambient. For these points of view, alloying with Ti may be a promising means to improve the characters of Cu interconnect.

However, as a interconnect material, the electrical characteristics of Cu–Ti alloy [referred to Cu(Ti) hereafter] are considered to be the most critical issue for practical applications. In this work, we have studies the leakage current characteristics of metal–oxide–semiconductor (MOS) structures made by deposition of Cu(Ti) alloy and pure Cu films on SiO₂/Si substrates. (Si) represents the single crystal wafer. In contrast to the high Ti contents in Cu(Ti) adopted in the literature studies (mostly greater than 10 at %), the Ti content in the current work is only 0.02 wt % so that the massive increase of resistivity and formation of Cu–Ti intermetallic compounds may be avoided. Material characterization of the Cu(Ti)/SiO₂/Si and Cu/SiO₂/Si multilayer structures are also performed to find out the correlation between the leakage characteristics and the interfacial reaction.

To address these concerns, Cu and Cu(Ti) films were deposited by magnetron sputtering on (100) Si wafers covered with 270 nm of thermal SiO₂. The Cu(Ti) films were co-sputtered from a Cu target (99.99% purity) and a Ti target (99.99% purity) with Ar plasma. The thicknesses of Cu and Cu(Ti) are 170 nm and 150 nm, respectively. By using electron probe microanalyzer (JEOL 8900R), the Ti content in Cu(Ti) is determined to be about 0.02 wt %. After deposition, Cu(Ti)/SiO₂/Si and Cu/SiO₂/Si were annealed at temperature ranging from 500 °C to 700 °C for 30 min in a vacuum, at a pressure of 2×10⁻⁵ Torr.

Film resistivity was calculated from the sheet resistance measured by a four-point probe and the film thickness measured by a Tencor α-step profilometer. Characteristic phases in the samples, before and after annealing, were determined by using θ–2θ x-ray diffraction [(θ–2θ XRD), Rigaku D-Max-IV] with Cu Kα radiation. Compositional depth profile analysis was performed by Auger electron spectrometry (AES), VG AES-310D and characteristic chemical bondings at interface were examined with x-ray photoelectron spectroscopy (XPS), VG ESCA 210. For MOS capacitor structures, Cu and Cu(Ti) films were used as the gate electrodes. The electrode dots were 500 μm in diameter and formed by lift-off process. Current–Voltage (I–V) curves were measured by using HP4140 picoammeter/dc voltage source with the electric field swept from zero to 1 MV/cm.

Figure 1 shows the resistivity of Cu and Cu(Ti) films as

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a function of annealing temperature. The as-deposited Cu and Cu(Ti) have resistivity values about 1.97 μΩcm and 3.89 μΩcm, respectively. It is known that the addition of other metals to Cu increases its resistivity and addition of 1 at % Ti raises the resistivity to 17.7 μΩcm.12 Also, high defect density and large surface-to-volume ratio of thin films will increase the resistivity. For that reason, the resistivity value for the as-deposited Cu(Ti) is conceivable. After annealing at 500 °C–700 °C, resistivity values of both systems decrease, but the reduction is more significant for Cu(Ti). The resistivity of annealed Cu(Ti) is lowered to ~2.5 μΩcm, which is rather low for Cu alloy films. Lowering of the resistivity may be attributed to two factors: annihilation of defects and segregation (or outdiffusion) of alloy content. The small drop in resistivity of the pure Cu film suggests that defect annihilation may have a relatively minor effect on the decrease of resistivity upon annealing. Therefore, the Ti content of the Cu(Ti) film can diminish upon annealing possibly by segregation to the interface (or free surface). Accordingly, the film resistivity will be considerably lowered. To prove this proposition, interfacial characteristics of the samples are examined as follows.

Regarding the presence of phase(s), θ–2θ XRD reveals diffraction peaks of Cu only for both systems, as deposited and after annealing at 500 °C–700 °C. No Cu–Ti compound is detected and Cu peaks for both systems are at the same position and have comparable widths. The observation is reasonable since the Ti content (only 0.02 wt %) is substantially below its solid solubility in Cu (which is ~0.6 wt % at 500 °C).13 However, to further investigate the Cu(Ti)/SiO2 and Cu/SiO2 interfaces, we have stripped the Cu(Ti) and Cu layers of the as-deposited and 700 °C annealed samples by chemical solution (mixture of nitric acid, phosphoric acid, and acetic acid). The exposed SiO2 surface was than examined by using XPS (Fig. 2). No Ti signal was detected at the as-deposited Cu(Ti)/SiO2 interface [Fig. 2(a)]. On the contrary, Ti 2p signals corresponding to TiO2 bonding was observed at the Cu(Ti)/SiO2 interface after annealing at 700 °C [Fig. 2(b)]. Because the Ti:O composition may not be exactly 1:2, the layer is designated as a TiO2 layer. As a comparison, no Ti signal was detected at the Cu/SiO2 interfaces [Figs. 2(c) and 2(d)] of the as-deposited and 700 °C annealed Cu/SiO2/Si samples.

It is reported that Ti can react with SiO2 to form a TiO2/ Ti3Si3 structure and the reaction is driven by the reduction of overall free energy.14 Therefore, SiO2 behaves as a strong sink and Ti additives in Cu(Ti) film will segregate to the interface and form TiO2. A similar result has been observed by Adams et al.5 They reported that in the Cu(27 at %Ti)/SiO2 system, Ti segregated to the Cu(Ti)/SiO2 interface and formed TiO2 after annealing at 500 °C (or above) in NH3. Our experiment demonstrates that even with a very low content, the Ti additives will migrate to the interface and form TiO2. Observation of TiO2 at the Cu(Ti)/SiO2 interface confirms the proposition that reduction of Cu(Ti) resistivity upon annealing is a result of Ti segregation. A similar mechanism for reduction of resistivity was also observed in Cu(1 at % Al)5 and (Cu 2 at % Mg)6 alloy systems. However, in these studies, oxides (Al2O3 and...
Cu(Ti)/SiO$_2$ / annealing at 700 °C due to the low Ti content in Cu than for the Cu system. Therefore, the formation of TiO$_x$ will improve the current leakage character between Cu and SiO$_2$, as indicated by the AES compositional depth profiles of Cu/SiO$_2$ / MgO) of the alloying elements were reported to form on the film surfaces and the annealings were carried out in Ar ambient.

The consequence of TiO$_x$ formation on the interfacial diffusion is shown by the AES compositional depth profiles of Cu/SiO$_2$/⟨Si⟩ and Cu(Ti)/SiO$_2$/⟨Si⟩ samples after annealing at 700 °C (Fig. 3). The Ti signal cannot be detected due to the low Ti content in Cu(Ti) film. One can see that the slopes of Cu and O profiles are more steep for Cu(Ti) system than for the Cu system. Therefore, the formation of TiO$_x$ at the Cu(Ti) interface [Fig. 2(b)] has the effect in preventing the Cu–SiO$_2$ interdiffusion. In other words, the self-formed TiO$_x$ layer behaves as a diffusion barrier. Because Cu is applied for interconnect metallization but not for contact metallization, this self-formed TiO$_x$ barrier layer does not need to be conductive. To reveal whether the TiO$_x$ barrier layer will improve the current leakage character between Cu and SiO$_2$, $I–V$ measurement on MOS capacitors were performed.

Figure 4 presents the $I–V$ curve of Cu/SiO$_2$/⟨Si⟩ and Cu(Ti)/SiO$_2$/⟨Si⟩ MOS capacitors, before and after annealing at 700 °C. The MOS capacitors with as-deposited Cu and Cu(Ti) gates exhibit about the same leakage current ($\sim 10^{-8} \text{ A/cm}^2$). Nevertheless, at electric field above 0.7 MV/cm$^2$, the leakage current of the Cu MOS is larger than Cu(Ti) MOS. In view of that, the as-deposited pure Cu is less resistant to the electrical force than Cu(Ti), and some copper atoms in the pure Cu may be driven into SiO$_2$ at high electrical field. After annealing at 700 °C, MOS capacitors with a Cu gate exhibit a rapid rise in leakage current at a low electrical field, indicating that massive diffusion of Cu into SiO$_2$ had occurred during annealing. On the contrary, the leakage current of 700 °C annealed Cu(Ti) MOS structure increases only by one order of magnitude as compared to the MOS with as-deposited Cu(Ti) gate. The result reflects that the Cu(Ti)/SiO$_2$ system has a superior reliability to the Cu/SiO$_2$ system. As revealed by the XPS and AES analyses (Fig. 2 and 3), low leakage current of Cu(Ti) MOS structure can be attributed to the formation of TiO$_x$ at the Cu(Ti)/SiO$_2$ interface, which inhibits the Cu diffusion into SiO$_2$ during annealing.

In conclusion, by investigating the electrical and material properties of Cu(Ti) alloy and pure Cu films deposited on SiO$_2$/⟨Si⟩, we have found the formation of a TiO$_x$ layer at the Cu(Ti)/SiO$_2$ interface upon annealing in a vacuum. This layer may serve as a diffusion barrier in preventing Cu diffusion into SiO$_2$ and significantly improves the electrical reliability. In addition, due to segregation of Ti to the interface and low Ti content (only 0.02 wt %), the Cu(Ti) layer exhibits an adequately low resistivity (2.5 μΩ cm) after annealing. Therefore, Cu (0.02 wt % Ti) can be a suitable metallization material for the ULSI interconnect system.

This work was supported by the National Science Council of Taiwan, R.O.C. (Contract No. NSC-89-2216-E-006-037).