Insights to the Scaling Impact on Back-Gate Biasing for FD SOI MOSFETs

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Abstract—This work investigates the scaling impact on the feasibility of back-gate biasing for ultra-thin-body and BOX fully depleted SOI MOSFETs (UTBB FD SOI) at 5nm technology node. Though the effectiveness of the threshold voltage ($V_t$) modulation by back bias is limited due to bulk inversion as a result of silicon film scaling, such an issue of reduced $V_t$ window can be relieved by decreasing BOX thickness as the back-gate coupling could be enhanced by thin-BOX-reduced inversion charge centroid in scaled SOI film.

Keywords—FD SOI, ultra-thin body and box (UTBB), back bias.

I. INTRODUCTION

While the nonplanar multi-gate MOSFETs are emerging, FD SOI continues to be competitive in prolonging the technology roadmap due to good control of short-channel effects (SCEs), simpler process and flexibility of using back-gate bias ($V_{GB}$) for $V_t$ tuning. However, the back bias technique becomes less effective when the SOI film thickness continues to be reduced to meet scaling requirements as bulk inversion becomes prevalent in thin silicon film. When the inversion charge distributes along the entire channel instead of being confined at surface, the back-gate coupling effect is weakened. This work provides insights to the scaling impact on back-gate biasing for understanding and overcoming the fundamental limits.

II. DEVICE SIMULATION AND DEVICE DESIGN

A. Simulation of UTBB FDSOI

According to the 5nm technology node of ITRS 2015, the nominal UTBB SOI in our study (Fig. 1) is designed with gate length ($L_G$) = 12nm, equivalent oxide thickness (EOT) = 0.6nm, silicon film thickness ($T_{Si}$) = 5nm, buried oxide thickness ($T_{BOX}$) = 10nm and gate work function tuned to meet the off-current ($I_{off}$) = 1nA/μm [1]. In addition, the undoped channel is used to reduce the process variation and increase the drive current. The highly doped ground plane (GP) beneath the buried oxide minimizes the depletion region that reduces the coupling effect [2]. To account for carrier confinement in the ultra-thin silicon film, the density gradient model is included in numerical device simulations [3].

B. Device design option

Since SCEs are associated with silicon film and buried oxide, they should be properly chosen. Drain-induced barrier lowering (DIBL) can be controlled with scaled $T_{BOX}$ and highly doped GP by suppressing the penetration of the fringing electric field [4], as shown in Fig. 2(a)). With sufficiently thin $T_{Si}$, the subthreshold swing (SS) increases as $T_{BOX}$ decreases due to smaller contribution of front gate capacitance (1-D effect). On the contrary, the lateral electrical field becomes apparent and can be suppressed with thin $T_{BOX}$ when $T_{Si}$ approaches $L_G$, such that SS starts to decrease with $T_{BOX}$ decreasing [5] (2-D effect), as shown in Fig. 2(b).

III. BACK-GATE BIAS TECHNIQUE

The flexibility of the back bias technique is explored herein for UTBB SOI at 5nm technology. When a forward bias is applied to the back gate, the threshold voltage, defined at a constant current, is lowered due to coupling from the back gate [6] [7]. Fig. 3 demonstrates the operation of available back gate bias within the range of $V_{DD}$. When a larger $V_t$ tuning range is needed, a more complicate peripheral circuit is needed to provide a larger $V_{GB}$ beyond $V_{DD}$. It is essential to maintain the design window of $V_t$ tuning from node to node.

![Fig. 1. Conceptual schematic of FDSOI (not to scale).](image1)

![Fig. 2. (a) DIBL and (b) SS vs. BOX thickness for different silicon film thicknesses.](image2)

![Fig. 3. Operation of available back gate bias.](image3)
which can be defined with a coupling factor \[8\]:

\[ r = \frac{3\text{EOT} + x_c}{3\text{TBOX} + \text{Tsi} - x_c} \]  

where \( x_c \) is the inversion charge centroid position which is linked to quantum confinement and cannot be ignored in thin SOI film even at zero back bias. When a forward bias is applied to the back gate, \( x_c \) moves toward the mid-film and virtually increases the EOT and decreases the silicon film. Fig. 5 shows that \( x_c \) increases with back bias, resulting in larger coupling effect, especially for thicker TSi.

TBOX contributes to back-gate coupling through BOX capacitance and implicit \( x_c \). As shown in Fig. 6(a), when TBOX is reduced, \( x_c \) is slightly reduced, and it is even further decreased if TSi is scaled. Such a decreasing trend of \( x_c \) tends to lower the coupling factor, as indicated in (1), and eventually disables the back-gate biasing. However, if TBOX is reduced sufficiently for device scaling, the TSi in (1) becomes predominant and scaling TSi becomes beneficial to back-gate coupling. To continue to maintain the \( V_t \) flexibility using back bias for 5nm node and beyond, TBOX should also be scaled accordingly.

Vt operation window is further evaluated when VGB is limited to VDD. Fig. 4(a) shows the tunable Vt window which decreases with TSi scaling. Since TSi scaling is needed for good control of SCEs, this work seeks to make sure that TBOX can not only enhance the Vt tuning window but also reverse the dependence on TSi thinning TBOX for the thinnest TBOX. The physical insights to this viable scaling strategy are discussed next.

The sensitivity of Vt to VGB reflects the coupling effect which can be defined with a coupling factor \[8\]:

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**REFERENCES**


