A 40-110 GHz High-Isolation CMOS Traveling-Wave T/R Switch by Using Parallel Inductor

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Outline

- Motivation and introduction
- MMW CMOS T/R switch: design procedure (in 90-nm CMOS)
- Simulation & measurement results
- Performance comparison
- Conclusion
- References
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Motivation and introduction

- **Application for millimeter-wave**
  - 57-64 GHz unlicensed band for wireless personal area network (WPAN) wireless video area network (WVAN)
  - 77 GHz bands for automotive radar
    - Automotive cruise control (ACC), Collision warning (CW), Anti-collision (AC) and Lane change assist (LCA)
  - For 94 GHz applications
    - MMW imaging radar for concealed weapons detection [1]
    - Medical imaging applications [2][3]
    - Imaging and gesture recognition [4]
Motivation and introduction

- **T/R switch in MMW RF transceiver:**
  - **T/R switch** connects **antenna**, **PA** and **LNA**

- **Design considerations:**
  - Low insertion loss
    - Reduce burden of the gain on **LNA** or **PA**
  - High isolation
    - Reduce **leakage signal** from the transmitter
  - High power handling
    - High \( IP_{1\text{dB}} \): avoid **power saturation**
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MMW CMOS T/R switch: design procedure

- Broadband CMOS MMW high-isolation T/R switch schematic
  - **Shunt inductor**: improve isolation
  - **Traveling-wave concept**: increase operation bandwidth
  - **Body floating**: reduce insertion loss
  - **Matching network**: improve return loss
Trade off in traveling-wave SPST switch design[5]:

- **Switch off** (MOS transistors in triode region):
  - MOS transistors are equivalent to **resistors**
  - more traveling-wave SPST stages → **isolation**↑ (Appendix)

- **Switch on** (MOS transistors in cut off region):
  - MOS transistors are equivalent to **capacitance**
  - more traveling-wave SPST stages → **insertion loss**↑

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Series T/R switch with parallel-inductors:
- The **LC tank** equivalent to a high impedance: reduce leakage signal (high isolation)
- narrow-band response

By adopting traveling-wave stage after the series switch:
- more traveling-wave SPST stages → **isolation & bandwidth**↑
**MMW CMOS T/R switch: design procedure**

- **SPDT switch design and operation:**
  - Parallel-shunt inductor is chosen as **154 pH @ 109 GHz**
  - For insertion loss and isolation, traveling-wave stage is chosen **n=2**

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**Graphs:**
- **Insertion loss**
  - Single resonated switch
  - Resonated switch with traveling wave, n=1
  - Resonated switch with traveling wave, n=2
  - Resonated switch with traveling wave, n=3
  - Resonated switch with traveling wave, n=4

- **Isolation (dB)**
  - Single resonated switch
  - Resonated switch with traveling wave, n=1
  - Resonated switch with traveling wave, n=2
  - Resonated switch with traveling wave, n=3
  - Resonated switch with traveling wave, n=4
**MMW CMOS T/R switch: design procedure**

- **Matching networks:**

  ✓ 40 -110 GHz: **return loss > 10 dB.**

  **Matching Network**

  - Step 1: No matching circuit
  - Step 2: Add series transmission line
  - Step 3: Add shunt-open stub
  - Step 4: Add pad

  ![Graphs showing return loss from 40 to 110 GHz](image)

- **Return loss graphs:**

  - Ant. return loss from 40 to 110 GHz
  - Output return loss from 40 to 110 GHz

- **Design Procedure:**

  1. Step 1: No matching circuit
  2. Step 2: Add series transmission line
  3. Step 3: Add shunt-open stub
  4. Step 4: Add pad
The designed T/R switch is fabricated with TSMC 90-nm CMOS technology

- A multi-layer structure (1P9M)
- To achieve low conductor loss
  - The signal path and matching elements are arranged on M9 (thick top metal)
- To prevent currents from injecting into the lossy substrate
  - The ground plane is placed at the bottom metal (M1)
A 40-110 GHz High-Isolation CMOS Traveling-Wave T/R Switch by Using Parallel Inductor

Chip size: $0.67 \times 0.4 \text{ mm}^2 (\approx 0.27 \text{ mm}^2)$
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Simulation & measurement results: (1)

Frequency range: 40 – 110 GHz

Simu.
Return loss: > 10 dB
Insertion loss: < 4 dB
Isolation > 21 dB

Meas.
Return loss: > 10 dB
Insertion loss: < 4 dB
Isolation > 20 dB (56 dB @ 109 GHz)
Simulation & measurement results: (2)

-Insertion loss (dB)

Input power (dBm)

- Tx to Rx isolation (dB)

Input power (dBm)

**Frequency at 94 GHz**

**Simu.**

$IP_{1\text{dB}} \text{ @ } 94 \text{ GHz} = 12 \text{ dBm}$

Isolation = 40 dB @ 15 dBm

**Meas.**

$IP_{1\text{dB}} \text{ @ } 94 \text{ GHz} = 10 \text{ dBm}$

Isolation = 34.2 @ 15 dBm
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### Performance comparison

**A 40-110 GHz High-Isolation CMOS Traveling-Wave T/R Switch by Using Parallel Inductor**

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<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>Process</td>
<td>90-nm COMS</td>
<td>90-nm COMS</td>
<td>45-nm COMS SOI</td>
<td>0.13-µm SiGe</td>
<td>90-nm CMOS</td>
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<td>Switch Topology</td>
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<td></td>
<td>SPDT</td>
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<td>Design Approach</td>
<td>Traveling wave</td>
<td>Transmission line integrated</td>
<td>Double shunt</td>
<td>Double shunt</td>
<td>Traveling wave</td>
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<td>Frequency range (GHz)</td>
<td>50 – 94</td>
<td>60 – 110</td>
<td>140 - 220</td>
<td>96 – 163</td>
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<td>60–110</td>
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<tr>
<td>Return loss (dB)</td>
<td>&gt; 10</td>
<td>&gt; 15</td>
<td>&gt; 10</td>
<td>&gt; 10</td>
<td>&gt; 10</td>
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<td>Insertion loss (dB)</td>
<td>&lt; 3.4</td>
<td>3 – 4</td>
<td>3-5</td>
<td>2.6 - 3</td>
<td>&lt; 4</td>
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<td></td>
<td>3.5 @ 94 GHz</td>
<td>&lt; 4</td>
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<tr>
<td>Isolation (dB)</td>
<td>&gt; 27</td>
<td>&gt; 25</td>
<td>&gt; 20</td>
<td>&gt; 23.5</td>
<td>&gt; 20</td>
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<td></td>
<td>(30 @ 94 GHz)</td>
<td>(27 @ 94 GHz)</td>
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<td>&gt; 27</td>
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<td>56 @ 109 GHz</td>
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<tr>
<td>Input P_{1dB}(dBm)</td>
<td>15 @ 77 GHz</td>
<td>10.5 @ 75 GHz</td>
<td>---</td>
<td>17 @ 94 GHz</td>
<td>10 @ 94 GHz</td>
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<tr>
<td>Chip size / Core size (mm²)</td>
<td>0.24 / 0.14</td>
<td>0.3 / 0.2</td>
<td>0.29 / 0.10</td>
<td>0.37 / 0.23</td>
<td>0.27 / 0.11</td>
</tr>
</tbody>
</table>
Conclusion

- A 40-110 GHz High-Isolation CMOS Traveling-Wave T/R Switch by Using Parallel Inductor is fabricated in 90-nm CMOS technology.
  - Chip size / Core size: 0.27 / 0.11 mm²
  - Measured insertion loss less than 4 dB @ 40-110 GHz and 3 dB @ 94 GHz
  - Measured Tx-Rx isolation better than 20 dB @ 40-110 GHz, 56 dB @ 109 GHz

- Wide bandwidth and high isolation can be achieved by traveling-wave topology with parallel inductors.

- The designed 40-110 GHz traveling-wave T/R switch has compact size and high isolation.
References


Thank you for your attention
Appendix
90-nm Transmission line model

- Ansoft HFSS EM tools:

Passivation layer (PASS)

- Top Metal: M9
- Multiple: M8
- Dielectric: M7
- Layers: M6
- Ground plane: M5
- Poly: M4
- Lossy Substrate: M3
- M2

![Diagram of transmission line model](image)

![Graph showing inductor (pH) vs. frequency (GHz)](image)
**Traveling-wave SPST structure analysis**

- **SPST switch off: (isolation)**
  - **ABCD matrix Analysis:**
    \[
    \begin{bmatrix}
    A_1 & B_1 \\
    C_1 & D_1
    \end{bmatrix} = \begin{bmatrix} 1 & Z_1 \\
    Y_1 & Y_1Z_1 + 1
    \end{bmatrix}
    \]
    \[
    \begin{bmatrix}
    A_2 & B_2 \\
    C_2 & D_2
    \end{bmatrix} = \begin{bmatrix} 1 & Z_1 \\
    Y_2 & Y_2Z_1 + 1
    \end{bmatrix}
    \]
    \[
    \begin{bmatrix}
    A_3 & B_3 \\
    C_3 & D_3
    \end{bmatrix} = \begin{bmatrix} Y_3Z_1 + 1 & Z_1 \\
    Y_2 + Y_3 + Y_2Y_3Z_1 & Y_2Z_1 + 1
    \end{bmatrix}
    \]

- For \( n = 3 \)

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
A_1 & B_1 \\
C_1 & D_1
\end{bmatrix} \begin{bmatrix}
A_2 & B_2 \\
C_2 & D_2
\end{bmatrix} \begin{bmatrix}
A_3 & B_3 \\
C_3 & D_3
\end{bmatrix} = \begin{bmatrix}
A_1 & B_1 \\
C_1 & D_1
\end{bmatrix} \begin{bmatrix}
A_2 & B_2 \\
C_2 & D_2
\end{bmatrix} \begin{bmatrix}
A_3 & B_3 \\
C_3 & D_3
\end{bmatrix}
\]

\[
Z_1 = j\omega L, Y_1 = \frac{1}{R_{on}} + j\omega C_l
\]

\[
Y_2 = \frac{1}{R_{on}} + 2j\omega C_l, Y_3 = j\omega C_l
\]
Traveling-wave SPDT structure analysis [5]

**Effective bandwidth:**
1. Return loss > 10 dB
2. Isolation > 20 dB
3. Insertion loss < 4 dB

Fig. 16. Complete schematic of an SPDT traveling-wave switch using the series HEMT switches ($M_1$ and $M_6$).

Fig. 11. Calculated: (a) insertion loss and (b) isolation of a three-transistor SPST traveling-wave switch with various number of transistors.
**Traveling-wave SPDT structure analysis**

- **Effective bandwidth:**
  1. Return loss > 10 dB
  2. Isolation > 20 dB
  3. Insertion loss < 4 dB
Traveling-wave SPDT structure analysis

**effective bandwidth:**
1. Return loss > 10 dB
2. Isolation > 20 dB
3. Insertion loss < 4 dB
Back up slides
Reviews of published works

- **Reported MMW SPDT switch:**
  - (a) Traveling-wave with $\lambda/4$ transformer [7]; (Chao et al, MWCL 2007, 50-94 GHz)
  - (b) Series-shunt with leakage cancellation [10]; (Kuo et al, RFIC 2011, 57-64 GHz)
  - (c) Single-shunt with $\lambda/4$ transformer [11]; (Uzunkol et al, JSSC 2010, 50-70 GHz)
**Body-floating technique** [12]

- The parameters will influence insertion loss: $R_B$, $R_{ON}$ & $C_T$

\[
\text{Insertion Loss} = \frac{1}{|S_{21}|^2} = \frac{(R_{ON} + 2Z_0)^2 + \omega^2 C_T^2 \left[ (R_{ON} + 2Z_0)R_B + (R_{ON} + Z_0)Z_0 \right]^2}{(2Z_0)^2 \left[ 1 + \omega^2 C_T^2 R_B^2 \right]} \]

\[
C_T = C_{DB} + C_{SB} + \frac{C_{GD} + C_{GS}}{C_{GD} + C_{GS} + C_{GB}} \]

**Body-floating technique [12]**

- A high resistor $R_B$ is connected to the body terminal of transistor and ground.
- High impedance path $R_D + R_B \Rightarrow$ *insertion loss improvement*

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**Experimental Results**

- **Insertion loss v.s $R_B$**

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![Graph showing insertion loss vs $R_B$](image-url)
Measurement setup: S-parameter

S-parameters measurement setup:

- This setup can only measure:
  (not included insertion loss and antenna return loss)

  1) Isolation (small signal)
  2) Tx. Rx return loss

* The insertion loss measurement setup will be discussed in the following sections.
Measurement setup: S-parameter

S-parameter measurement setup
**Measurement setup: IP$_{1dB}$ & insertion loss**

- **IP$_{1dB}$, Insertion loss measurement setup**
  - *different measurement setup from S-parameters.*
  - For measuring switch high IP$_{1dB}$: need power amplifier after SG
  - The harmonic Mixer $P_{out, max} = -10$ dBm: require the attenuator
Measurement setup: $\text{IP}_{1\text{dB}}$ & insertion loss

- $\text{IP}_{1\text{dB}}$, Insertion loss measurement setup
IIP3 measurement setup:

* different measurement setup from S-parameters.

- **Two tone test**: need two signal generators.
- The harmonic Mixer $P_{out, max} = -10$ dBm (require the attenuator)
## Simulation & measurement results summary

### 40 – 110 GHz CMOS T/R Switch (TSMC 90-nm GUTM CMOS)

<table>
<thead>
<tr>
<th></th>
<th>Simulation results</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range</td>
<td>40–110 GHz</td>
<td>40–110 GHz</td>
</tr>
<tr>
<td>Vc (high / low) (V)</td>
<td>1.2 / 0</td>
<td>1.2 / 0</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Output return loss (dB)</td>
<td>&gt; 10.3</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Ant return loss (dB)</td>
<td>&gt; 11.1</td>
<td>Could not be measured</td>
</tr>
<tr>
<td>Insertion loss (dB)</td>
<td>&lt; 4</td>
<td>&lt; 4</td>
</tr>
<tr>
<td></td>
<td>3.6 @ 94 GHz</td>
<td>3 @ 94 GHz</td>
</tr>
<tr>
<td></td>
<td>4 @ 109 GHz</td>
<td></td>
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<tr>
<td>Port-isolation (dB)</td>
<td>&gt; 21 (40–110 GHz)</td>
<td>&gt; 21 (40–110 GHz)</td>
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<tr>
<td></td>
<td>&gt; 27(60–110 GHz)</td>
<td>&gt; 27(60–110 GHz)</td>
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<tr>
<td></td>
<td>40 @ 94 GHz</td>
<td>36 @ 94 GHz</td>
</tr>
<tr>
<td></td>
<td>47 @ 109 GHz</td>
<td>56 @ 109 GHz</td>
</tr>
<tr>
<td>Input P₁dB (dBm) @ 94 GHz</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>IIP3 (dBm) @ 94 GHz</td>
<td>23</td>
<td>20.2</td>
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<tr>
<td>Die size</td>
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