Abstract—A 40-110 GHz SPDT T/R switch fabricated in 90 nm CMOS is presented. The traveling wave switch is used to obtain low insertion loss and wide operating bandwidth. To enhance the isolation performance, the parallel inductor is adopted. The insertion loss is improved with body-floating. The measurement results show that the insertion loss is lower than 4 dB and isolation is better than 21 dB. A very good isolation value higher than 56 dB at 109 GHz is achieved. The chip core size is 0.11 mm$^2$.

Index Terms—90-nm, 40-110 GHz, CMOS, high-isolation T/R switch, millimeter-wave (MMW), traveling wave

I. INTRODUCTION

Recently, Millimeter-wave (MMW) communication systems have tremendous developing potential and have many applications such as wireless personal area network (WPAN) around 57 – 64 GHz, automotive radar applications at 77 GHz and MMW radars for medical imaging and gesture recognition at 94 GHz [1][2]. In a MMW RF transceiver, the transmitter/receiver (T/R) switches with low insertion loss, high isolation and high power handling are required. Many MMW T/R switches are implemented with low insertion loss and high isolation by GaAS, HEMT process technology[3][4]. With the fast developing of CMOS process, system-on-chip (SoC) applications become mainstream for cost saving and highly integrated systems. However, CMOS lossy substrate will be a challenge for the switch design.

In general, the traveling-wave concept T/R switch is desired for MMW application due to low insertion loss and wide bandwidth response. However, there is tradeoff between insertion loss and isolation for traveling wave switches. Usually, high isolation and low insertion loss response may not be able to achieve simultaneously with traveling wave structure. In [5], the series-shunt structure with high isolation by using leakage cancellation technique is presented. Furthermore, parallel-shunt inductors are adopted to cancel NMOS parasitic effect to enhance switch isolation [6].

In this work, the parallel-shunt inductor is proposed in the design of a 40-110 GHz traveling-wave SPDT T/R switch. The designed switch is fabricated using the 90 nm CMOS technology. A wide bandwidth response is obtained, and both of high-isolation and low insertion loss are achieved.

II. CIRCUIT DESIGN

A. TRAVELING WAVE SPST DESIGN

The circuit schematic of the proposed 40–110 GHz traveling wave SPDT T/R switch with the body-floating technique and parallel inductor is shown in Fig. 1. The T/R switch is designed by applying two SPST traveling wave switches. The traveling wave stage can be designed by properly selecting the inductor’s value and transistor’s size, Fig. 2(a) shows the equivalent circuit of the SPST switch when the transistors are off-state. The characteristic impedance of the artificial transmission line is

$$Z_0 = \sqrt{\frac{L}{C_{off}}} \quad (1)$$

$C_{off}$ is the off-state capacitance of the transistors(M3-M6). In the proposed switch design, $L_3$,$L_4$ is chosen as 60 pH and transistors’ width (M3-M6) are chosen as 26 um.

For the SPST switch isolation, Fig. 2(b) shows the equivalent circuit when the transistors are on-state. It can be observed that transistors are equivalent to small resistors, and the SPST circuit is equivalent to a small resistance path. The simulated results of different traveling wave sections are shown in Fig. 3. It can be observed that there is tradeoff between isolation and insertion loss. The more traveling wave sections (n), the better switch isolation performance can be obtained. However, the insertion loss is deteriorated by limited-Q inductors and transistor’s parasitic effect. Hence, the traveling wave stage numbers (n) will be carefully chosen and discussed in the following section.

B. SPDT SWITCH SYNTHESIS

The SPDT traveling-wave switch employing the series switch is reported in [4]. In order to improve the isolation performance, the parallel inductors ($L_1$,$L_2$) is applied to series switch (M1,M2). When the series switch (M1,M2) is in off-state, the parasitic capacitance is resonated with parallel inductor at resonance frequency ($f = \frac{1}{2\pi \sqrt{LC}}$). Thus, the isolation response is improved. Moreover, the isolation can be further improved by increasing the traveling wave stage [4].
When the transistors of traveling wave SPST switch are in on-state, the leakage signal is led to ground by multiple shunt resistors. However, as mentioned above, the insertion loss is deteriorated with multiple traveling wave stages. Simulation results of SPDT switch using parallel inductor with different traveling wave sections ($n$) is shown in Fig. 4. In considering the trade off between insertion loss and isolation, the width of the series switch ($M_1,M_2$) is chosen as 36 um, the parallel inductor is chosen as 154 pH and traveling wave SPST switch stage is chosen as $n=2$ at the resonating frequency of 109 GHz. In order to further improve insertion loss response, matching circuits are adopted to the antenna (Ant), transmitter (Tx) and receiver (Rx) ports. For size reduction, all the microstrip lines of matching networks are meandered. Also for EM coupling consideration, all circuit has been simulated by the full-wave HFSS EM simulators.
parallel-shunt inductors are employed. The measured results show high linearity. To achieve the high isolation performance, a floating technique is adopted to achieve low insertion loss and high isolation. The T/R switch is fabricated in 90-nm CMOS technology. The return loss are better than 10 dB. The input $P_{1dB}$ is 10 dB, is obtained without sacrificing other switch performance. Also, a low insertion loss performance, which is less than 4 dB, and the highest isolation value is 56 dB at 109 GHz. The switch chip size and core size is 0.27 mm$^2$ and 0.11 mm$^2$, respectively.

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## REFERENCES


### TABLE I  PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th>Process</th>
<th>Design Approach</th>
<th>Frequency range (GHz)</th>
<th>Return loss (dB)</th>
<th>Insertion loss (dB)</th>
<th>Isolation (dB)</th>
<th>$IP_{1dB}$ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs HEMT</td>
<td>Traveling wave</td>
<td>20-135</td>
<td>10</td>
<td>4</td>
<td>&gt; 27</td>
<td>15 @ 77GHz</td>
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<td>90 nm</td>
<td>Traveling-wave integrated</td>
<td>60 – 110</td>
<td>&gt; 15</td>
<td>2</td>
<td>27</td>
<td>7 @ 94GHz</td>
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<td>90-nm CMOS</td>
<td>Traveling wave</td>
<td>50-110</td>
<td>&gt; 10</td>
<td>3</td>
<td>&gt; 27</td>
<td>15 @ 94GHz</td>
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<td>15 @ 94GHz</td>
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**III. MEASUREMENT RESULTS**

The CMOS T/R switch is fabricated in the 90-nm CMOS process. As shown in Fig. 5(a), the insertion loss is lower than 4 dB, and the return loss is better than 10 dB, respectively. Fig. 5(b) shows that the isolation is better than 35 dB at 94 GHz and 56 dB at 109 GHz, respectively. Fig. 6 shows the measured $IP_{1dB}$ is 10 dBm at 94 GHz. Furthermore, the isolation performance at different input power at 94 GHz has been investigated and shown in Fig. 7. The chip size of proposed SPDT switch is 0.27 mm$^2$ and the core size is 0.11 mm$^2$, the chip micrograph is shown in Fig. 8.

Table I summarizes the measured performance comparison. Compared with reported MMW SPDT switches, the good high isolation performance of the proposed switch can be observed. The highest isolation value is 56 dB at 109 GHz. Also, a low insertion loss performance, which is less than 4 dB, is obtained without sacrificing other switch performance. The return loss are better than 10 dB. The input $P_{1dB}$ is 10 dBm at 94 GHz.

**IV. CONCLUSION**

A 40 - 110 GHz CMOS high-isolation traveling wave T/R switch by using parallel inductor is presented. The SPDT switch is fabricated in 90-nm CMOS technology. The body floating technique is adopted to achieve low insertion loss and high linearity. To achieve the high isolation performance, parallel-shunt inductors are employed. The measured results