ABSTRACT
As the number of buses in multi-core SoC designs increase, bus planning problems become a dominant factor in determining the chip performance. To cope with these issues, it is desirable to consider them in the early floorplanning stage. Recently, many bus-driven floorplanners have been proposed in the literature. However, those proposed algorithms only consider the bus planning problem without the thermal effect. As a result, there are hotspots which result in high chip temperature on the chip. In this paper, a thermal-aware bus-driven floorplanning algorithm is proposed to separate hotspots during the perturbation stage and to keep buses away from hotspots during the routing stage. To avoid time-consuming thermal simulations, the superposition of thermal profiles which are the thermal distribution of each module is adopted to efficiently estimate the module temperature. Compared with the state-of-the-art bus-driven floorplanner, experimental results demonstrate that the proposed algorithm can effectively separate hotspots and reduce the chip temperature.